

MST® Dopant Blocking for Advanced 3D Applications

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Introduction

Advanced 3D devices for the 2/3nm node, such as nanosheets, gate-all-around (GAA) and other structures, build on existing bulk FinFET manufacturing technology. The requirements for managing abrupt interfaces, with steep doping profiles, are becoming increasingly stringent. Atomera's MST® technology can be used to control dopant diffusion in layers thinner than 5nm, meeting key requirements for advanced 3D devices.

Brief History of the FinFET

Early research into a forerunner of the FinFET, the DELTA transistor, was pioneered by Digh Hisamoto and co-workers at Hitachi's Central Research Laboratory from 1989 [1]. Hisamoto then joined a 1997 DARPA project at UC Berkeley with Prof. Chenming Hu, Prof. Tsu-Jae King-Liu and other researchers, including Atomera's own Hideki Takeuchi. This team demonstrated the first deep sub-micron N- and P-FinFETs as well as the first FinFET utilizing a high-k metal gate (HKMG) dielectric, which is now the industry-standard approach [2-4]. The term FinFET was coined in 2000 [3] because the vertical silicon channel resembles a shark's fin (see Fig. 1).

In 2011 Intel launched the first commercial FinFET (Tri-gate transistor) at the 22nm node [5]. Foundries, such as TSMC, Samsung and Global Foundries followed with their own versions at the 16/18nm node from 2014. Many of the early research FinFETs borrowed from silicon-on-insulator technology to eliminate the body connection from source to drain and isolate the vertical fin channel. The Intel 22nm FinFET and all subsequent commercial FinFETs, however, use bulk silicon substrates. High doping is required beneath the fin to reduce leakage from punch-through, as illustrated in Figure 1.

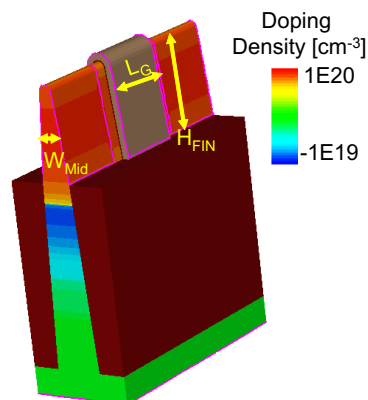


Fig. 1. 3D schematic of 22nm FinFET. High body doping $\sim 1\text{E}19 \text{ cm}^{-3}$ of opposite polarity to the source and drain doping is required to prevent punch-through leakage

From bulk FinFETs to Nanosheets and other advanced 3D devices

Bulk FinFETs require a sharp vertical transition from high body doping of one polarity to even higher doping of opposite polarity in the source-drain region. In the fin channel, underneath the gate, it is preferable to have low doping. So once again, a sharp vertical transition is required, this time from high body (anti punch-through) doping to low doping in the channel. In practice, the thermal steps of the manufacturing process lead to dopant diffusion, and a more gradual transition between the doping regions. Out-diffusion of the high source-drain doping leads to a reduction in doping and hence an increase in source/drain series resistance, reducing the current that the FinFET can provide. Up-diffusion of the body doping into the lightly doped fin channel can reduce the carrier mobility and hence the current, and is also a source of parametric variability from random dopant fluctuation (RDF). The high source-drain doping can also diffuse laterally into the fin channel. To minimize these deleterious effects, the bulk FinFET manufacturing process temperatures are reduced compared to planar nodes (22nm and above), and various other processing steps are introduced. But dopant diffusion remains a constraint on the scalability and processing costs of FinFETs.

Advanced 3D devices for the 2/3nm node appear likely to build on FinFET technology, as they further sub-divide the fin channel into a vertically-stacked series of thin nano-sheets. One example, from a recent announcement by IBM [6], is shown in Figure 2.

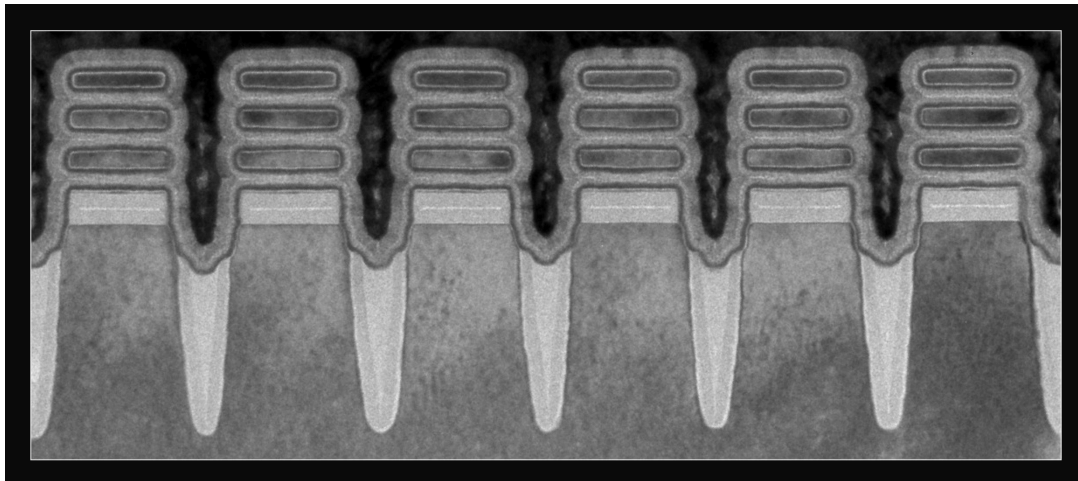


Figure 2. (taken from IBM's recent 2nm announcement). The vertical fin is now sub-divided into a series of parallel nanosheets, which offer higher current and better control. Intel and leading Foundries are following similar (though differentiated) approaches.

Similar issues around dopant diffusion remain, and in fact are even more stringent. In addition to the need to eliminate punch-through in the bulk silicon below the nanosheets, it is important to keep the very high source/drain doping from diffusing into the nanosheets. Germanium diffusion also needs to be minimized, when Si / SiGe layers are grown for nanosheet formation.

As we shall see, MST can reduce the underlying causes of dopant diffusion and hence simplify the manufacturing process as well as improve performance and variability.

How dopant diffusion can impair FinFETs and advanced 3D devices

Intel 22nm and 14nm 3D TCAD models

To quantify the ways in which dopant diffusion can impair bulk FinFETs, Atomera commissioned a study by Prof. Suman Datta. Prof. Datta previously worked at Intel, leading the development of the Intel HKMG solutions and working on the early Intel FinFET (Tri-gate) program before moving to Pennsylvania State University and then the University of Notre Dame. The major findings were published in joint publications with Atomera staff [7,8].

3D TCAD models were developed by Prof. Datta and his team, which closely replicated the published I-V characteristics of the Intel 22nm and 14nm devices [5]. Figure 3 shows the comparison of the modeled I-V and the published experimental data from Intel. Figure 4 shows the doping transitions in two vertical cross-sections: the first from the source/drain region into the body and the second from the fin channel into the body.

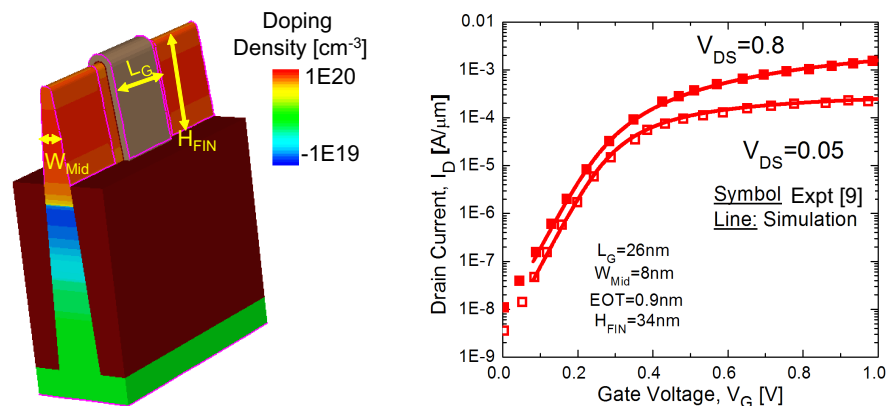


Fig. 3. (a) 3D schematic of 22nm FinFET; (b) 3D numerical device simulations are in excellent agreement with the experimental 22nm FinFET [5].

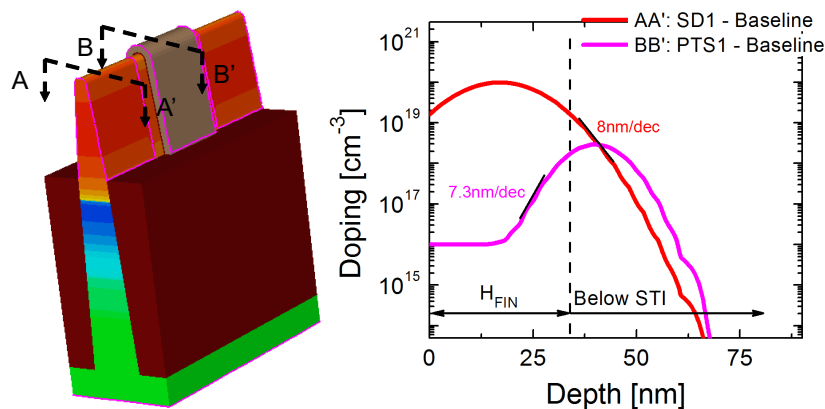


Fig. 4 Extracted dopant profile for baseline Si FinFET: Source/Drain (S/D) profile (SD1: baseline) and Punch-through Stopper Implant profile (PTS1: baseline)

The 3D TCAD models enable simulation of the effect of reducing diffusion, to maintain higher doping in the source/drain and to make a steeper transition in the channel region. For example, making a more abrupt transition from the high punch-through stop doping in the body, to the low channel doping was found to have a significant effect, both on the I-V characteristics and on the variability. Changing the doping gradient (see the BB' cut in Fig. 4.) from the baseline value of 7.3nm/decade to a more abrupt 3.3nm/decade (emulating MST) was found to increase the I_{dsat} and I_{dlin} by 7% and 13% respectively. Other electrical parameters were unchanged or also slightly improved.

As explained previously, a dopant diffusion blocking layer below the fin channel can also block the out-diffusion of the source/drain doping. When this effect is modeled in conjunction with the up-diffusion blocking of the punch-through stop implant, even more dramatic improvement can be seen. The combined effect of reducing the up-diffusion of the punch-through stop and reducing the out-diffusion of the source/drain leads to a 10% increase in I_{dsat} and a 21% increase in I_{dlin} .

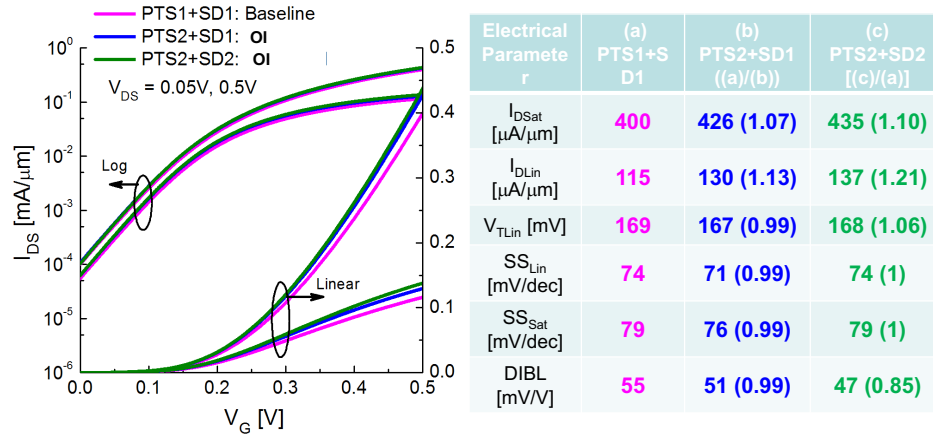


Fig. 5. Transfer characteristics of (a) baseline 22nm FinFET; (b) reduced up-diffusion punch-through stop (PTS2 + SD1) 22nm FinFET and (c) combined reduction of source/drain out-diffusion and up-diffusion blocking (PTS2 + SD2) FinFET.

One of the prime sources of parametric variability in advanced devices is from what is known as random dopant fluctuation, or RDF. The devices have such a small volume that only a few dopant atoms difference can make a significant change to the threshold voltage and hence the I-V characteristics. Stray dopant atoms from diffusion can thus cause significant variations in device performance, and hence the range of values that need to be taken into account in the circuit design. The reduced diffusion FinFETs analyzed above also exhibit reduced RDF and overall reduced V_t variability, as seen in the table in Fig. 6. Reducing the overall variability allows a tighter specification over the manufacturing range. Since leakage depends exponentially on V_t , the net result is an ability to lower the median V_t , allowing yet higher median current. Conversely, the same current can be achieved for a lower supply voltage. Since power dissipation depends on the square of the supply voltage, this reduction in variability can be used to reduce power.

Device	$\sigma_{V, Th-RDF}$ (mV)	$\sigma_{V, Th-LG}$ (mV)	$\sigma_{V, Th-LEP}$ (mV)	$\sigma_{V, Th-HFIN}$ (mV)	$\sigma_{V, Th-EOT}$ (mV)	$\sigma_{V, Th-WF}$ (mV)	$\sigma_{V, Th-Total}$ (mV)	% of RDF contribution
SD1+PTS1: Baseline	19.98	3.6	18	3.2	10	12.4	31.6	40
SD1+PTS2: OI	15.24	4.8	16	0.2	7.5	12.4	26.8	32
SD2+PTS2: OI	14.22	4.8	16	0.2	7.5	12.4	26.3	29

Fig. 6. Considering RDF fluctuation as well as geometric fluctuation, the reduced diffusion FinFETs show 17% improvement in $\sigma_{V, Th-Total}$ over the baseline 22nm FinFET.

Overall, it can be seen that there are significant advantages to reducing dopant diffusion in bulk FinFETs – almost a “generation” of drive current enhancement as well as significant variability reduction, which can in turn enable reduced power. Because of the evolution of advanced 2/3nm devices from FinFET manufacturing technology, these benefits are also relevant to future devices.

How MST reduces diffusion

The introduction of oxygen (and other elements) in the MST manufacturing process is designed to maintain the silicon (semiconductor) lattice so that high-quality epitaxial growth is sustained. A few Angstroms above or below a given inserted oxygen layer it is expected that the silicon lattice is identical to regular silicon. In the immediate vicinity of the inserted oxygen, however, the silicon lattice has to distort slightly to accommodate the additional element(s), and because of the electro-negativity of the oxygen there is also some local charge transfer, which again is negligible a few Angstroms away from the inserted layer. An idealized model is shown in Fig. 7.

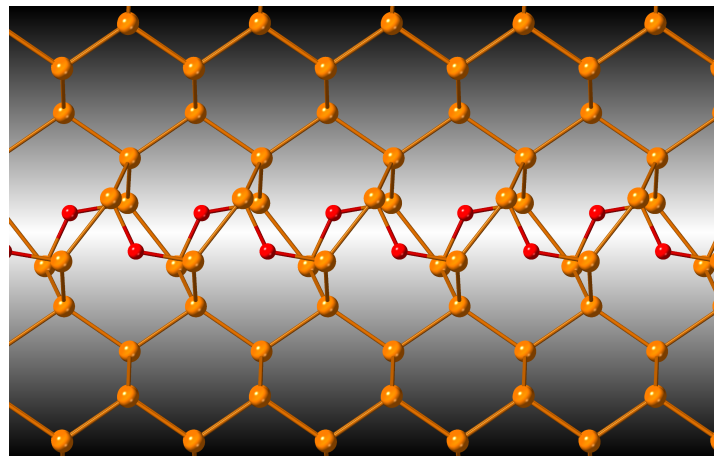


Fig. 7. Idealized model of a MST oxygen layer in a silicon lattice. Note the distortion in the immediate vicinity of the (red) oxygen layer.

The local distortion / charge perturbation leads to local minima for substitutional dopants, such as boron or phosphorus and also for point defects: silicon self-interstitials and vacancies. Thus the MST oxygen layer can be used to block a flux of interstitials and trap electrical dopants (which remain substitutional). Atomera has invested considerable resources to characterize these interactions and then build them into TCAD models. In December of 2020 Atomera launched MSTcad, a set of tools for TCAD users of Synopsys Sentaurus™ platform. These TCAD tools now allow a wide range of MST-enabled devices to be modeled.

MST diffusion blocking data

Boron and phosphorus are well known to diffuse readily in silicon, particularly when they combine with silicon self-interstitials to form dopant-interstitial pairs. The MST oxygen layers are doubly effective at reducing diffusion, because they trap and localize the interstitials as well as trapping boron and phosphorus. Below, in Fig. 8, the effectiveness of MST to act as a “retaining wall” for phosphorus is shown for different anneals.

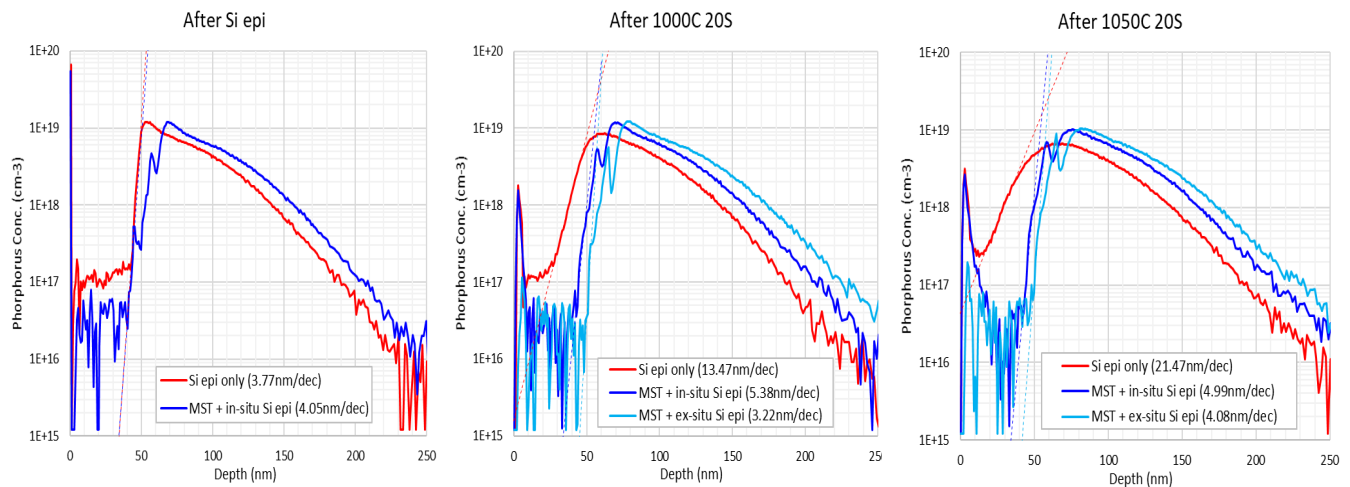


Fig. 8. Effectiveness of MST to maintain steep phosphorus profiles after 1000C 20s and 1050C 20s anneals. Note that the reduction of phosphorus diffusion also leads to a higher peak phosphorus doping, which is beneficial for source/drain applications

Similar effectiveness is shown for blocking of boron diffusion. The data are obtained by SIMS (secondary ion mass spectroscopy).

MST effectiveness compared to carbon doping

The main technique currently used by the semiconductor industry to reduce dopant diffusion, is to co-dope silicon with carbon. Carbon is a substitutional dopant (it sits in the same lattice location compared to where a silicon atom would normally sit). While the industry has tolerated carbon doping, it brings other issues of changing the silicon stress, and is recognized as a contaminant which can increase scattering and reduce current.

Carbon doping has been known for more than twenty years, and has been well characterized. The classic experiment/diagnostic for the effectiveness of carbon doping on diffusion blocking is a boron marker experiment. Boron is introduced during silicon, silicon-germanium or silicon-germanium-carbon epitaxial growth, typically as two thin regions: one without and one with carbon doping. Once grown the epitaxial stack is then subject to various anneals, and measured by SIMS.

A similar experiment can be performed by placing a thin MST layer between two in-situ boron-doped regions, as shown in Figure 9. The beauty of this technique is that it can be used quantitatively to compare diffusion under various anneals. In Figure 9, the silicon control simply has two thin boron-doped regions, the MST version adds a thin MST region separating the two boron-doped regions. Under an oxidizing anneal, as a gate oxide is formed, silicon self-interstitials are injected from the surface (at 0nm depth). Thus the top boron doped region is subject to an interstitial flux and freely diffuses. For regular silicon, it can be seen for a 850C 30min oxidizing anneal, the two boron ‘markers’ are almost completely diffused into each other. The MST layers, on the other hand, trap the injected interstitials and almost completely prevent diffusion of the lower marker. By changing the annealing conditions, such experiments can be used to calibrate the interstitial blocking as a function of temperature and gaseous ambient (oxidizing / inert). Looking closely at Fig. 9, it can also be seen that some boron is trapped between the two boron markers by the MST oxygen layers. These experiments can also be used to calibrate the boron trapping coefficient as a function of temperature and gaseous ambient

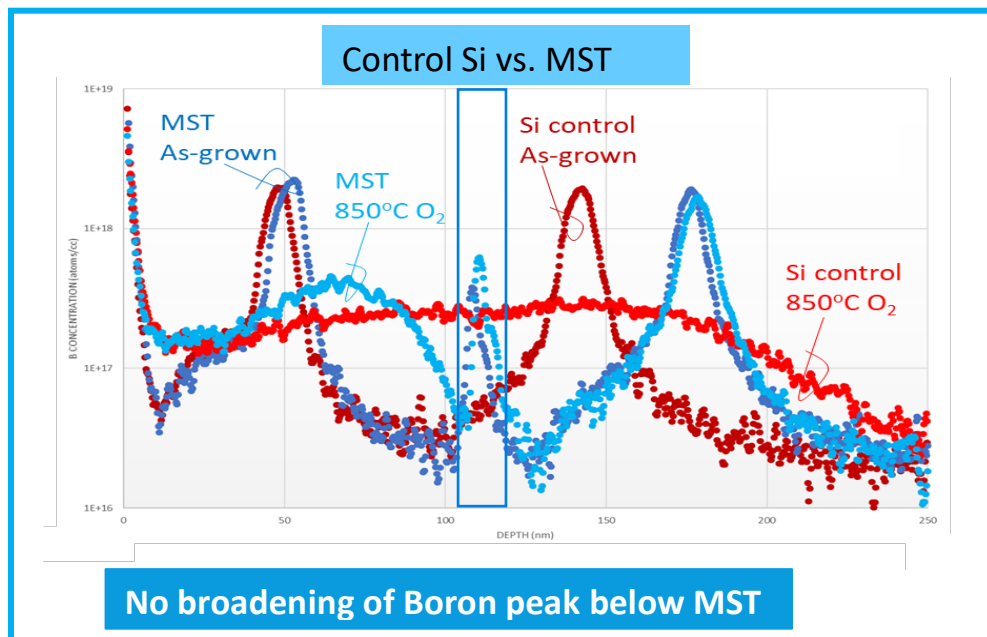


Figure 9. Boron marker experiment for oxidizing anneal (850C, 30min). The silicon-oxide interface is at 0nm and the MST layers are in the position marked by the blue box around 100nm depth. The dark red plot shows the as-grown boron markers separated by regular silicon. Under the 850C anneal, the bright red curve shows that the boron peaks are barely resolvable after undergoing significant diffusion. The dark blue curve shows the as grown marker separated by a thin MST region (in the blue box shown). After the 850C anneal the lower boron marker sees negligible diffusion, because of the highly effective trapping of silicon self-interstitials.

Comparing the MST boron marker with published data for SiGe:C (carbon doping) it can be seen, comparing Fig. 9 and 10, that MST is significantly more effective for the same thermal anneal. While the silicon control is similar in both experiments, for the SiGe:C case, the peak of the lower boron marker is reduced more than 3x, and the boron marker broadens by a factor of two, compared to almost no discernable change for MST in Fig. 9. Because of the quantitative nature of these experiments, the diffusion coefficient under carbon doping and MST can be directly compared. The result is that MST is more than twice as effective as carbon doping. Furthermore, as we shall see, the diffusion blocking can be achieved in a very thin epitaxially grown MST region, considerably broadening the application scope of the MST approach.

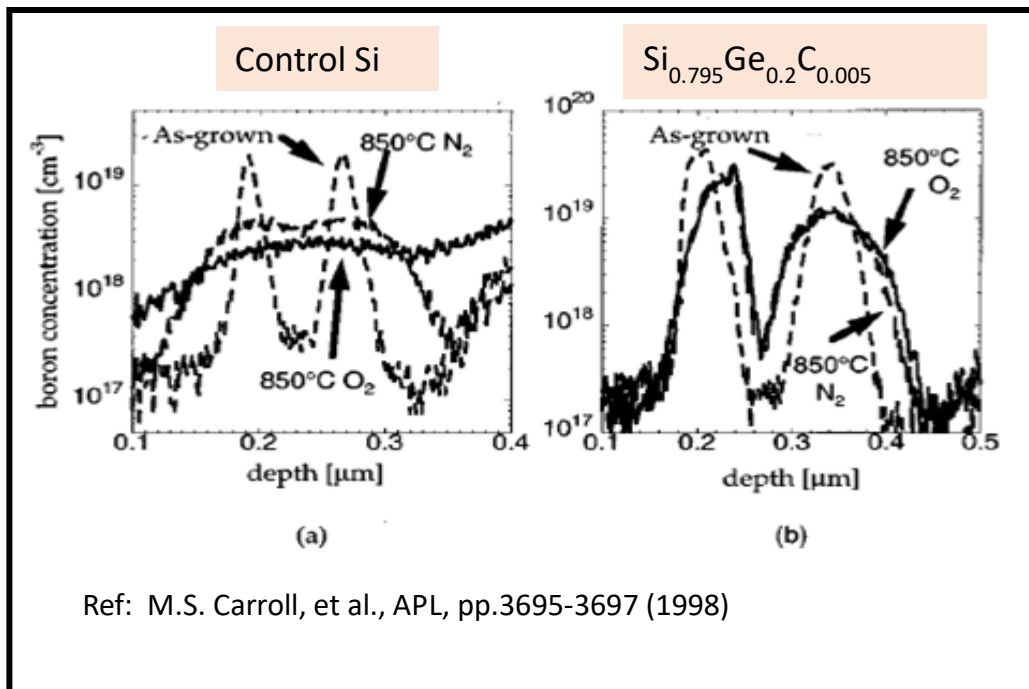


Figure 10. Published boron marker experimental data for SiGe:C

Latest MST diffusion blocking data

In Figures 8 and 9, the overall thickness of the grown MST silicon region was greater than 10nm (distance between top- and bottom-most oxygen layers). For the phosphorus doping in Fig. 8, the local trapping of doping at each oxygen layer, particularly the bottom-most layer, leads to a small spike, which can be seen by careful inspection of Fig. 8 around 60nm depth. The top 60nm silicon can form the starting material for FinFET or nanosheet formation. Further MST layers can also be inserted above the punch-through stop layers during nano-sheet formation.

For advanced 3D applications such as nanosheets/GAA it is desirable to further minimize the grown MST thickness, so that the sharpest doping transition can be achieved. Recent MST film development has targeted maintaining steep doping profiles with thinner grown MST.

Atomera uses two metrics to calibrate the effectiveness of the dopant blocking: the averaged gradient on the log plot (measured in nm/decade, as used above) and the overall percentage of dopant that “breaks through” the MST film, as integrated over the silicon region above the MST layers. Our goal for 2021 was to achieve >90% blocking for a grown MST region of less than 5nm. The Atomera epi team has risen to the challenge and excelled. The latest characterization data has shown 99% blocking (compared to silicon controls) of both boron and phosphorus for MST films thinner than 5nm, under 1000C 20s anneals, and 98% for 1050C 20s anneals. Atomera believes these data significantly increase the epi applications for MST in advanced devices.

Examples of the recent dopant blocking data are shown in Fig. 11.

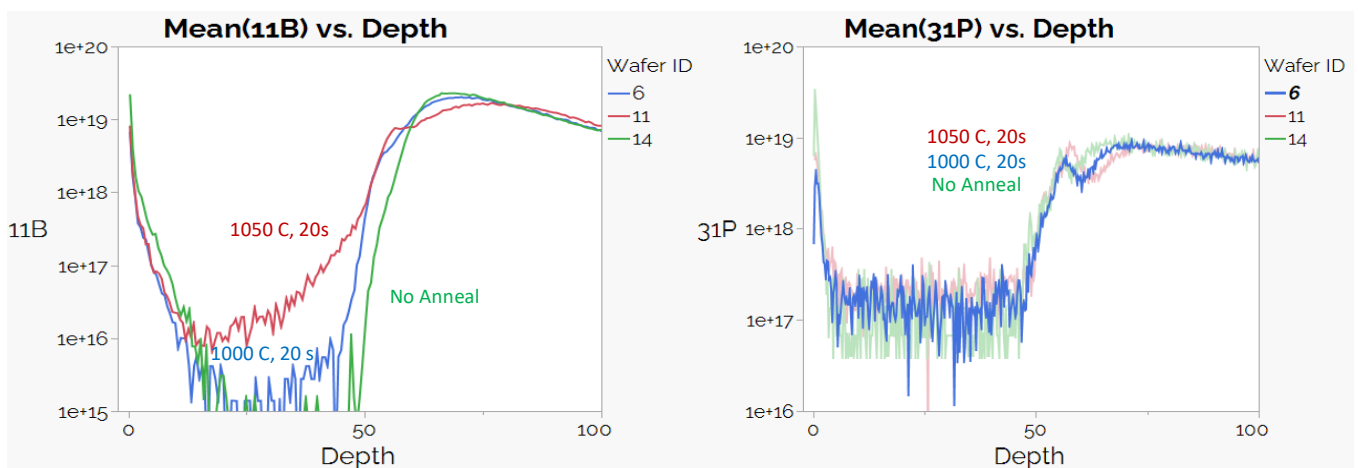


Figure 11. Boron and phosphorus dopant blocking for MST film of less than 5nm thickness. Compared to silicon control data, the integrated breakthrough doping is less than 1% for the 1000C, 20s anneal. The phosphorus doping is effective across both anneals because of even stronger trapping of phosphorus by the MST layers.

Conclusions

In summary, advanced 3D solutions down to the 2/3nm node such as nanosheets, GAA and other structures will need very effective doping control at a variety of interfaces. MST is an excellent candidate for controlling dopant diffusion and has been shown to be significantly more effective than carbon-doping, even for thin MST regions less than 5nm.

References

- 1) Hisamoto, Digh; Kaga, Toru; Kawamoto, Yoshifumi; Takeda, Eiji (December 1989). "A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET". *International Electron Devices Meeting*: 833–836.
- 2) Hisamoto, Digh; Hu, Chenming; Liu, Tsu-Jae King; Bokor, Jeffrey; Lee, Wen-Chin; Kedzierski, Jakub; Anderson, Erik; Takeuchi, Hideki; Asano, Kazuya (December 1998). "A folded-channel MOSFET for deep-sub-tenth micron era". *International Electron Devices Meeting*: 1032–1034.
- 3) Xuejue Huang, Wen-Chin Lee, Charles Kuo, Digh Hisamoto, Leland Chang, Jakub Kedzierski, Erik Anderson, Hideki Takeuchi, Yang-Kyu Choi, Kazuya Asano, Vivek Subramanian, Tsu-Jae King, Jeffrey Bokor, Chenming Hu (December 1999) "Sub 50-nm FinFET: PMOS" *International Electron Devices Meeting*: 67–70.
- 4) Daewon Ha, H Takeuchi, Y-K Choi, T-J King, WP Bai, DL Kwong, A Agarwal, M Ameen, (December 2004), "Molybdenum gate HfO₂ CMOS FinFET technology", *International Electron Devices Meeting*: 643-646.
- 5) C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neiryneck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," (2012) *Proceedings of VLSI Symposium on Technology*, pp. 131–132
- 6) See for example, <https://newsroom.ibm.com/2021-05-06-IBM-Unveils-Worlds-First-2-Nanometer-Chip-Technology,-Opening-a-New-Frontier-for-Semiconductors>
- 7) Robert J. Mears, Hideki Takeuchi, Robert J. Stephenson, Marek Hytha, Richard Burton, Nyles W. Cody, Doran Weeks, Dmitri Choutov, Nidhi Agrawal and Suman Datta, "Punch-through stop doping profile control via interstitial trapping by oxygen-insertion silicon channel", *Proc. IEEE Elect. Devices Technol. Manuf. Conf.*, pp. 65-66, 2017.
- 8) Hideki Takeuchi, Robert J. Mears, Robert J. Stephenson, Marek Hytha, Dan Connelly, Pavel Fastenko, Richard Burton, Nyles W. Cody, Doran Weeks, Dmitri Choutov, Nidhi Agrawal and Suman Datta, "Punch-through stop doping profile control via interstitial trapping by oxygen-insertion silicon channel", *IEEE Journal of the Electron Devices Society*, vol. 6, pp. 481-486, 2018, doi: 10.1109/JEDS.2017.2769682