

# Smoothing the Surface: MST® Turbo-Charges GAA Devices

*Robert Mears & Hideki Takeuchi*  
*Atomera, Incorporated*

## Outline

In this White Paper we outline some recent learning on Atomera's MST® technology and how it improves carrier mobility. We have discovered that MST reduces surface roughness scattering, and hence improves surface-roughness-limited mobility, by 55%. We believe that this result is important for doped and undoped devices operated at high vertical effective field, including leading edge gate-all-around (GAA) devices.

## Table of Contents

- Introduction
- MST Key Benefits Across Nodes
- MST Mobility Introduction
- MST Mobility Origins
- New Learning
- Scaling Significance
- MSTcad™ Implications and Simulation
- MSTcad Mobility Model
- Scaled Node Simulations
- MST HKMG Mobility Improvement versus Simulation
- Summary

## Introduction

We call our technology MST, which stands for Mears Silicon Technology. MST is “quantum-engineered” to enhance transistor performance, based on over 15 years of R&D. In our previous White Paper (MST for PMIC and RF SOI switches) we focused on the proven ability of MST to engineer doping profiles and thus enhance power switch devices. We have found that MST provides higher dopant retention and much steeper doping transitions for a wide variety of thermal processing conditions, enabling better device scaling and reduced mismatch.

In this paper we focus on MST's inherent improvement in carrier mobility and recent learning on the origins of this improvement. A single MST design improves both NMOS and PMOS devices, distinguishing its origins from strain engineering. By enabling “super-steep” retrograde vertical doping profiles the low-field mobility can be improved at matched  $V_t$  compared to regular control devices. We have found that MST also significantly improves high-field mobility. To better understand the origins of this high-field mobility we have performed detailed low temperature mobility measurements down to 4K. We have shown that the surface roughness component of mobility is improved by 55% compared to non-MST control devices.

## Smoothing the Surface: MST® Turbo-Charges GAA Devices

MST works across a wide technology space, from legacy planar nodes to the most advanced 3D applications. In essence MST gives you more drive current from the same device footprint. Compared to a given baseline, MST provides improved PPAC - power-performance-area/cost.

An existing semiconductor device will have some baseline operating point that is a compromise of speed, cost and power. Depending on the sector and customer we will typically trade-off the various benefits of the MST technology to provide higher speed, or reduced area and hence cost or reduced power, or some combination of all three!

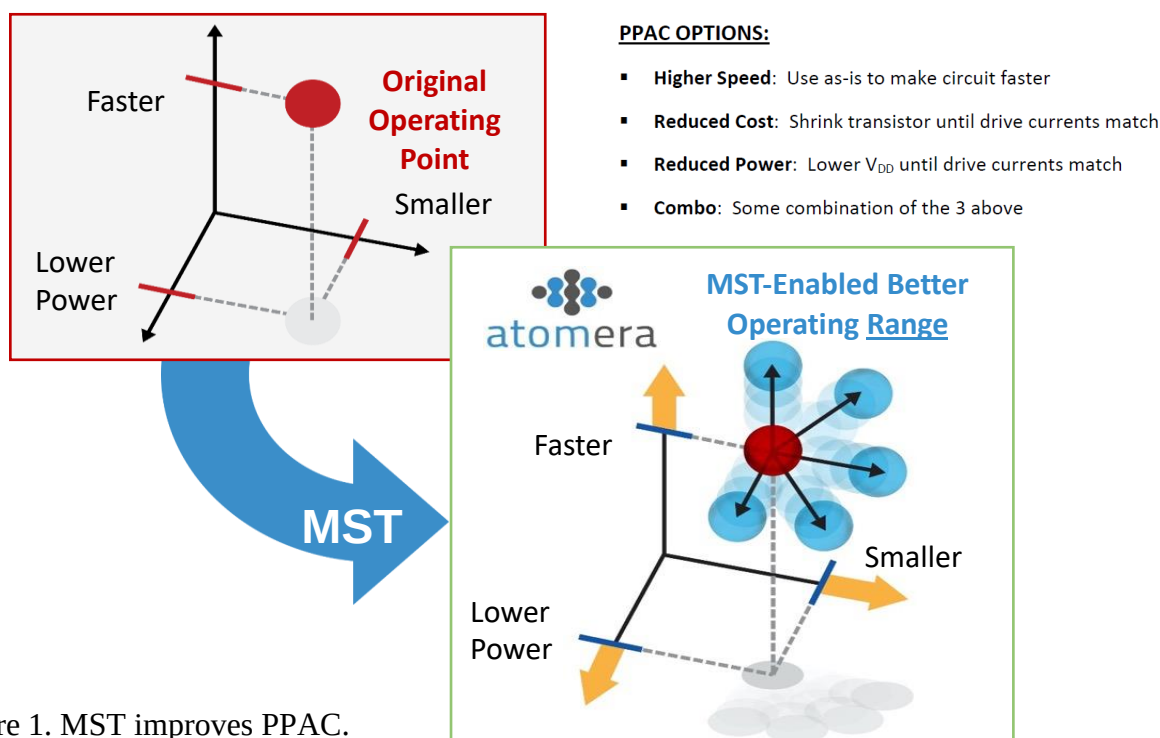


Figure 1. MST improves PPAC.

### MST Key Benefits Across Nodes

MST is applicable across a very wide technology space. Figure 2. shows the relative contributions of dopant engineering, mobility and reliability engineering, based on the combination of a variety of electrical device data and device modeling. We focus in this White Paper on the first row: Mobility (carrier mobility improvement). Note that the figure has been updated from our previous White Paper because of the new low-temperature data. For GAA devices the projected mobility is now >15% rather than <5% as previously projected.

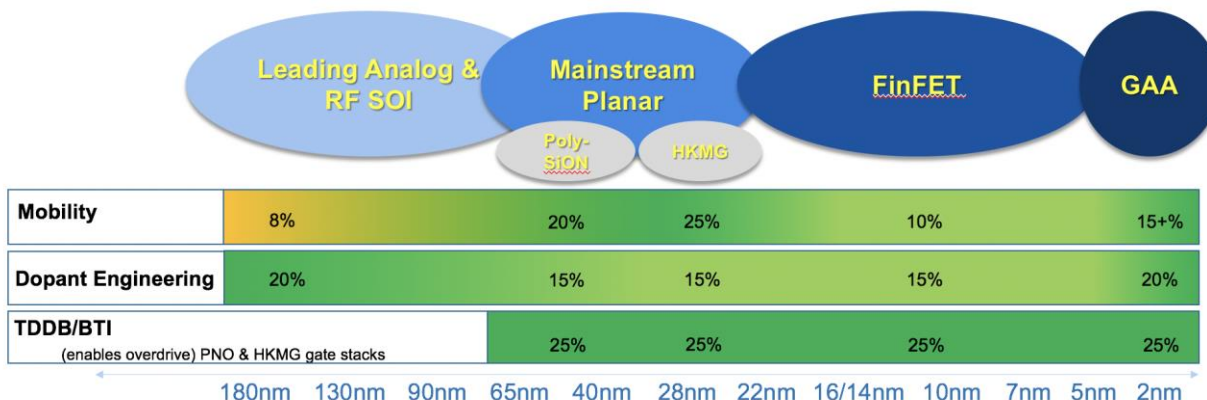


Figure 2. Key benefits of MST across different nodes.

## MST Mobility Introduction

The original value proposition for MST is based on the proven improvement of electron and hole mobility to provide enhanced conductivity. One of the key early results was that the same MST film design can improve both NMOS and PMOS devices, as shown in Fig. 3. This result clearly differentiates MST from strain engineering, in which tensile strain is required to improve NMOS while compressive strain is required to improve PMOS. Thus, different mechanical structures and even different materials are required for the strain engineering of CMOS devices. It turns out that MST can be used in addition to strain engineering to further improve device performance.

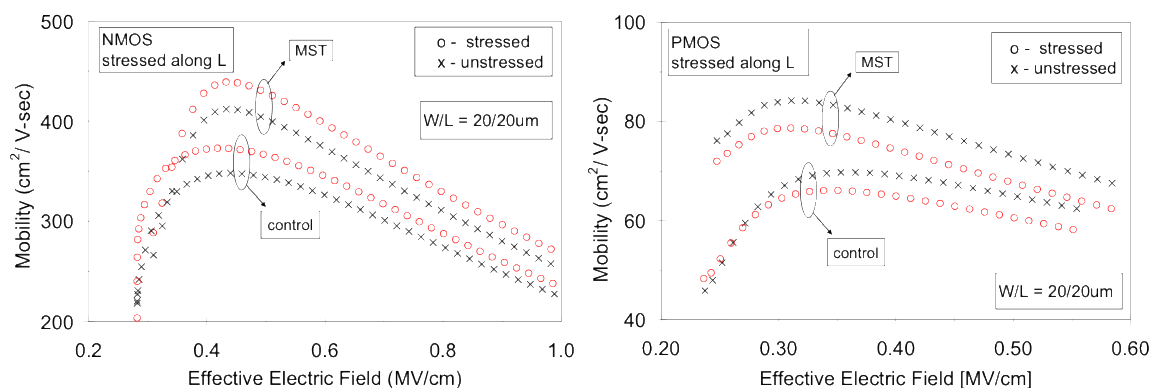


Figure 3. Early characterization of MST versus Control Mobility by Prof. Tsu-Jae King Liu and colleagues at UC Berkeley using a 130nm CMOS technology from ATDF.

Both NMOS and PMOS devices are enhanced with MST compared to non-MST Control devices. Tensile strain further improves NMOS devices, with similar piezo-coefficients for both MST and Control. By contrast tensile strain degrades both PMOS devices (compressive strain is needed to improve PMOS devices). The figures illustrate that MST improves both NMOS and PMOS, differentiating the mobility improvement from a strain-based effect. Strain engineering can be used

to further enhance the mobility improvement. Thus, MST is compatible and additive to strain engineering.

### **MST Mobility Origins**

While the MST mobility enhancement has been known for many years, the fundamental mechanisms behind the MST improvement have been less well understood. In general, there are many mechanisms which cause the scattering of electrons and holes. Basically, any deviation from a perfect (periodic) lattice causes scattering. For silicon devices, a famous 1994 paper by Shin-Ichi Takagi, who was at Stanford, and his colleagues from Toshiba, separated these mechanisms into three main components: Coulombic scattering (from dopants), Phonon scattering (from silicon lattice vibrations) and surface roughness scattering. It was found that the overall mobility of silicon samples prepared by different groups and using different fabrication techniques followed the same Universal behavior when plotted against the vertical effective electric field in the channel of the devices. The effective field is typically measured in MV/cm and depends on the thickness of the gate oxide and the threshold voltage,  $V_t$  as well as the operating point gate voltage. The early scaling laws of CMOS devices to achieve shorter gate lengths (and hence more transistors per unit area) drove thinner gate oxides (thinner from an electrical perspective), higher doping and lower voltages, but kept the effective field constant. For various reasons, primarily power, the threshold and operating voltages have proved harder to reduce. Thus, the operating point of most devices has moved to higher effective fields as technology is scaled.

Coulombic scattering reduces with increasing effective field, whereas phonon and surface roughness scattering increase. For the operating point of power and RF switches (well above  $V_t$ ), the mobility is typically dominated by phonon and surface roughness scattering. The relative Coulombic component is almost negligible. On the other hand, for devices operated below or close to the threshold voltage the Coulombic contribution can be quite significant.

One contribution to MST mobility improvement is readily understood in terms of Coulombic scattering. We can engineer MST devices with matched  $V_t$  but with fewer channel dopants near the gate oxide interface by using MST to block the up-diffusion of dopants during thermal processing to create a “super steep retrograde” (SSR) or “quasi-delta-doped” profile. Analog devices that are operated at close to  $V_t$  can take advantage of this mobility benefit. Also, high frequency devices that need high conductance close to  $V_t$  can be better engineered with MST.

But switches and logic devices are operated well above  $V_t$  where Coulombic scattering is less significant. Fortunately, MST also improves high-field mobility, and this is where our understanding has recently improved.

### **New Learning**

We had previously assumed that the MST high-field mobility improvement is because MST reduces phonon scattering, while surface roughness scattering was untouched, in keeping with

---

observed universal mobility behavior. Our breakthrough has come from detailed low-temperature characterization of MST mobility by Prof. Hiu-Yung Wong at San Jose State University. Prof. Wong is a device expert who was previously at Synopsys, and has worked with the Atomera team for a number of years. By cooling samples down to close to absolute zero (4 K or approximately -456 F), the lattice vibrations (and hence phonon scattering) are literally frozen out so that the only contributions to mobility are Coulombic and surface roughness scattering. To our surprise (and delight!), the relative mobility improvement of the MST samples compared to control samples only improved as the samples were cooled. By 4K MST improved both peak and high-field mobility by more than 50%! The measured samples were 5V thick-gate oxide devices fabricated at our partner facility TSI. Thus, at room temperature, where phonon scattering is dominant, the relative MST improvement was only about 10%. But detailed analysis confirmed that MST is indeed improving the surface scattering limited mobility by 55%, while phonon scattering is unaffected.

### **Scaling Significance**

The importance of this result is that more highly scaled, thin-gate devices operate at significantly higher effective fields, where surface roughness scattering is more limiting. Not only that, but for scaled planar devices the well doping level is also much higher and so the MST Coulombic improvement is better. Thus, much higher MST mobility improvement can be expected (~30%-50%), even at room temperature. Add to this the recent additional fundamental improvements observed for high-k metal gate devices and the MST value proposition is far stronger than we had originally expected.

For the most advanced nodes, the channel is substantially undoped, and so it is expected that the MST Coulombic benefit is negligible. For this reason, our recent focus has been on the many other ways MST dopant engineering can be used to improve such devices, by engineering abrupt doping interfaces, for example, in contacts, punch-through (leakage) stops or during the actual formation of nanosheets. But in addition, we can now project that MST, in conjunction with HKMG, can also bring higher mobility and hence higher performance metrics. We expect to be able to engineer more than a typical node's improvement in performance for a fraction of the development cost!

### **MSTcad Implications and Simulation**

For the past few years, Atomera has been working closely with Synopsys to develop an add-on capability to the Synopsys Sentaurus™ suite of TCAD tools, for modeling MST.

In the upper left of figure 4 it can be seen that the unique doping profiles enabled by MST are well-captured compared to physical SIMS (Secondary Ion Mass Spectroscopy). The doping profiles integrate into S-Device so that electrical parametrics can be simulated. As an example, in the lower left figure it can be seen that the  $V_t$  dependence on well dose is also closely modelled.

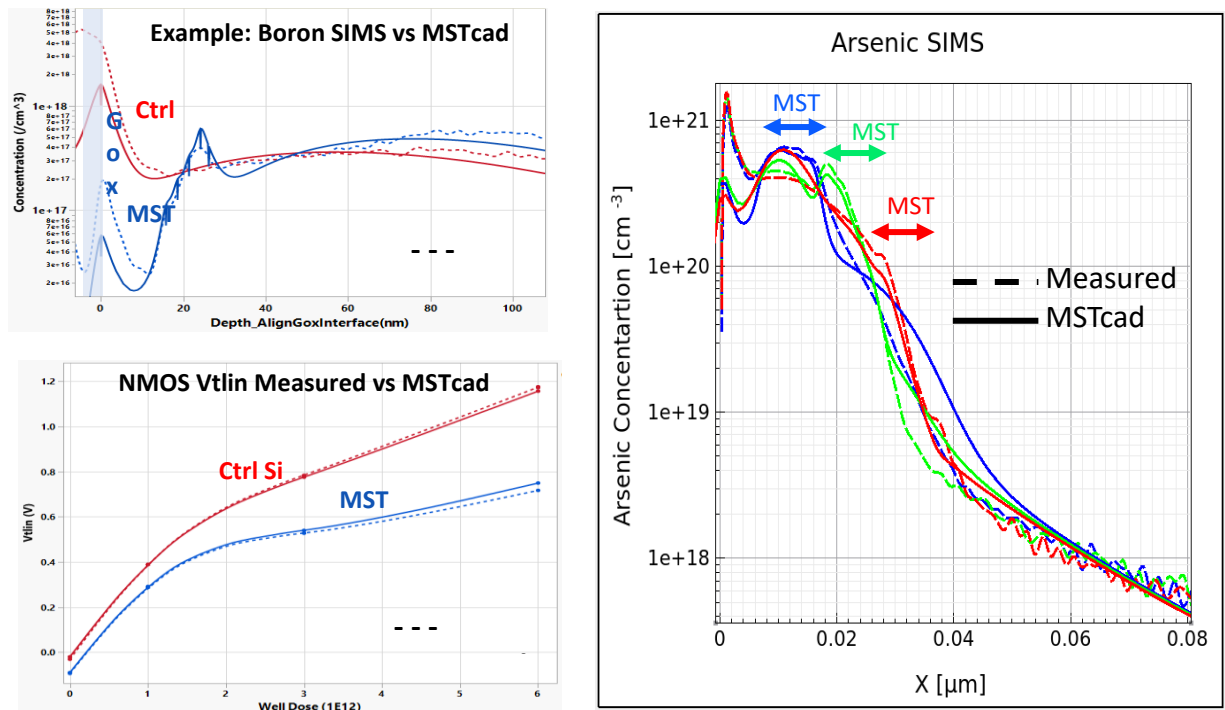


Figure 4. MSTcad™ Comparison with physical SIMS and electrically measured Vtlin.

## MSTcad Mobility Model

The Synopsys Sentaurus™ suite (SDevice) offers a number of different mobility models. Our preferred model is known as IALMOB, which has been particularly designed to model (I)nversion and (A)ccumulation (L)ayer (MOB)ility.

Because the unique dopant profiles enabled by MST are well-modelled by Sentaurus™ SProcess, as seen in Figure 4, the Coulombic contribution to mobility is automatically captured, provided that the doping profiles are correctly transferred to the device simulator, SDevice.

The simplicity of the new learning, is that the improvement in surface-roughness scattering can be directly included in the IALMOB coefficients, enabling fast and accurate assessment of MST mobility improvement for a wide variety of CMOS devices.

## Scaled Node Simulations

Although the precise fabrication details for Atomera's advanced node customers are closely guarded secrets, generic process conditions can be used to evaluate the MST impact on a variety of scaled process nodes. In fact, Synopsys already provide their user-base with worked examples of a variety of devices.

The new learning on surface roughness mobility can be directly transferred to simulation of planar devices with silica (SiO<sub>2</sub>) based dielectrics. However, it is known HKMG devices are significantly different, with other mobility degradation mechanisms arising from the polar nature of the high-k dielectric and other interface mechanisms. Additional scattering mechanisms such as soft phonon scattering, remote Coulomb scattering and remote roughness scattering have been proposed to account for the mobility degradation unique to HKMG stack.

Further low temperature characterization of HKMG devices is needed to better predict the MST mobility enhancement. But the new surface roughness model can be used to set a lower bound on the MST improvement, thanks to MSTcad modeling of our previous HKMG mobility data.

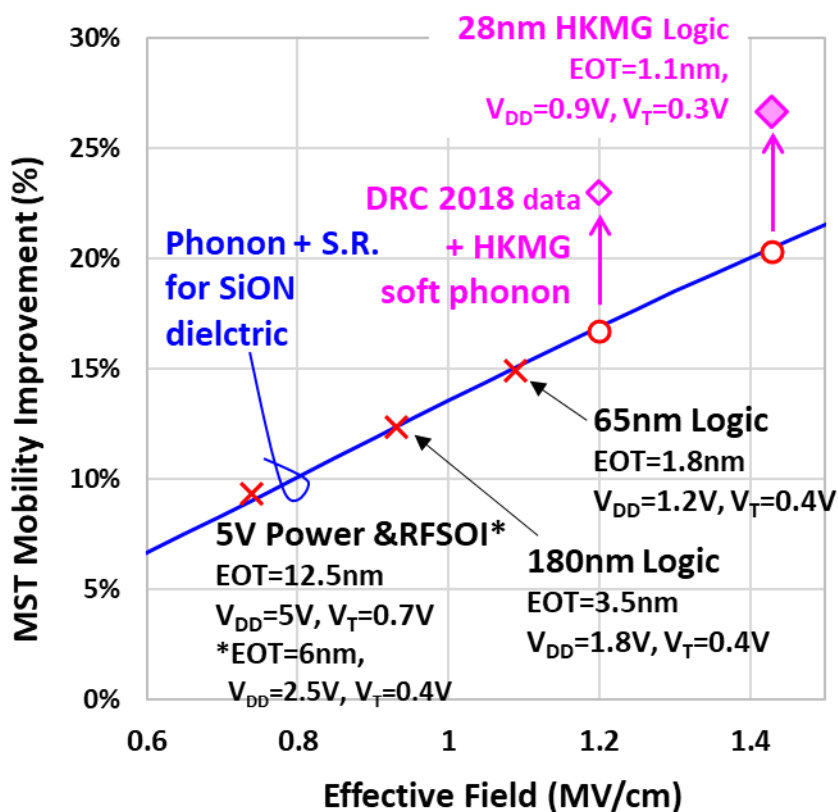


Figure 5. MST HKMG High Field Mobility Improvement versus Simulation.

We have previously published room temperature and limited over-temperature characterization of NMOS mobility for HKMG devices. This work was published jointly with Prof. Suman Datta and his team at the University of Notre Dame. Since we know the precise process details of these HKMG, we can apply the surface roughness model extracted from the low temperature SiO<sub>2</sub> data and compare it with experimental data. When we reviewed the electron mobility improvement of the HKMG gate stack devices, we found that the MST mobility improvement is >30% greater than the predicted poly-Si/SiON gate stack data at the same effective field. That there is additional MST mobility gain unique to HKMG stack is not surprising because we recently reported that MST modifies HKMG intermixing and the interface charge dipole in Journal of Applied Physics. Overall, this is very good news for MST on HKMG NMOS. The MST mobility improvement based on the new surface roughness model measured on SiO<sub>2</sub> dielectrics UNDERESTIMATES the overall MST mobility improvement for HKMG devices. Until the low temperature HKMG characterization is complete, we can still use the improved MST mobility model, on the understanding that the current model sets a lower bound for the overall mobility improvement.

### Summary

For the most advanced nodes, the channel is designed to be lowly-doped, and so it is expected that the MST Coulombic benefit is small. We previously projected an overall MST mobility benefit of <5%. Our recent focus for GAA has been on the many other ways MST dopant engineering can be used to improve such devices, by engineering abrupt doping interfaces, for example, in contacts, punch-through (leakage) stops or during the actual formation of nanosheets. But in addition, we can now project that MST, in conjunction with HKMG, can also bring >15% higher mobility for GAA and hence higher performance metrics. Because the overall MST mobility improvement increases with effective field, the MST mobility advantage is better maintained even in scaled nodes. We expect to be able to engineer more than a typical node's improvement in performance for a fraction of the development cost!