



White Paper: MST® Benefits for Gate-All-Around (GAA)

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Outline

In this White Paper we outline some recent learning about Atomera's MST® technology and how it can be used to improve advanced 3D devices, particularly gate-all-around (GAA) nanosheet devices (sometimes also called "RibbonFETs" or "Multi-Bridge Channel" (MBC) FETs). The key MST benefits for these devices are dopant diffusion control [1], improved mobility [2,3], the recently discovered work-function engineering potential of MST [4] and MST's ability to improve contacts by reducing the Schottky-barrier height [5].

Summary: This White Paper will show that MST can improve GAA devices in 4 ways:

- Creating enhanced Punch-Through Stop (PTS) layers
- Improving device mobility by ~15%
- Enabling thinner work function metals (WFMs) that reduce stacking height by 10%
- Reducing overall contact resistance by 11%.

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Introduction and Evolution of Advanced Nodes

We call our technology MST, which stands for Mears Silicon Technology. MST is "quantum-engineered" to enhance transistor performance, based on over 15 years of R&D. In our previous White Papers ("MST® for PMIC and RF SOI Switches" and "Smoothing the Surface: MST® Turbo-Charges GAA Devices") we focused on the proven ability of MST to engineer doping profiles and thus enhance power switch devices and our recent discovery that MST improves surface roughness scattering mobility. Both of these benefits also have specific applications in GAA devices.

In this paper we focus on GAA applications of MST. A single MST insertion can improve both NMOS and PMOS devices and there are multiple potential “insertion points” in a GAA flow. Epitaxial silicon / silicon-germanium growth is already established in GAA flows. Put simply, wherever there is an epitaxial step, it is highly likely that an MST epitaxy step can provide further benefit.

Transistor scaling is all about increasing the packing density of transistor switches while keeping power and power density under control. The power dissipation comes from active power (power during active switching) and passive power (off-state or “leakage” power). Reducing the operating voltage (V_{dd}) reduces active power (which is proportional to V_{dd}^2) and off-state leakage power, but also reduces the on-state current. Since the on-state current determines the speed of charging coupled devices, increased performance comes from *increasing* the on-state current, so there is a performance-power trade-off. The on-current can also be increased by making wider devices, but that comes with an area penalty, and hence packing density trade-off (cost). This is the basic PPAC (power-performance-area-cost) trade-off for semiconductor devices. The switching speed (clock frequency) also leads to increased active power. This is the main reason why processor architectures generally stopped increasing clock rates some years ago and moved to multi-core.

During the era of planar scaling, to keep the power manageable while shrinking the gate length, the effective thickness of the gate dielectric had to be reduced and the body doping had to be increased, in order to maintain a low-power off-state. The introduction of high- κ metal gate (HKMG) relaxed the physical thickness of the gate dielectric (which was contributing to significant leakage power) and provided improved on-off control. The evolution from planar to FinFET devices enabled the packing density to be increased by turning the transistors on their side, so that the planar width became the height. But gate-length scaling was still limited. The best control of the off-state is to have the gate all around the device, so that now, in the GAA era, multiple transistors are stacked on top of each other, as seen of the far right of Figure 1.

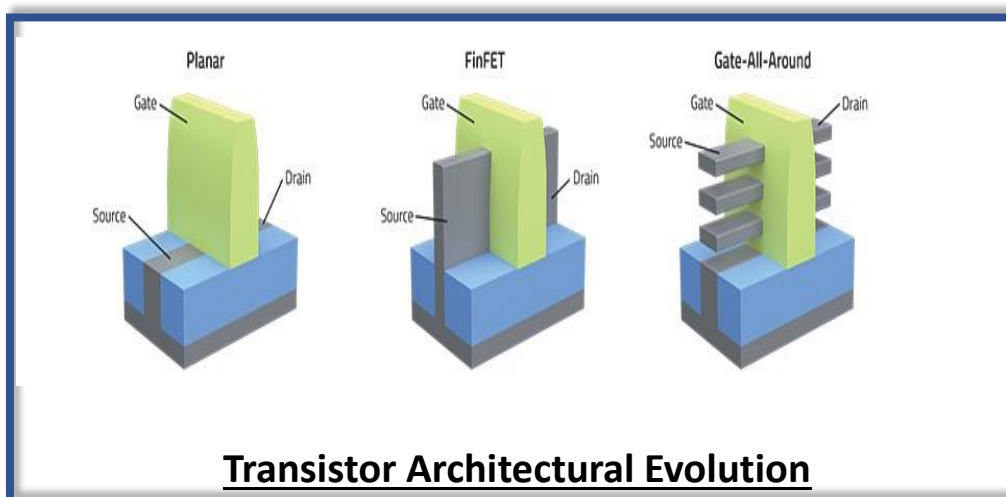


Figure 1: Evolution of transistors from planar, through FinFET to Gate-All-Around

In essence, and as we shall see in more detail, MST gives you more drive current from the same device footprint. Compared to a given baseline, MST provides improved PPAC - power-performance-area/cost. An existing semiconductor device will have some baseline operating point that is a compromise of speed, cost and power. Depending on the sector and customer we will typically trade-off the various benefits of MST technology to provide higher speed, or reduced area and hence cost or reduced power, or some combination of all three!

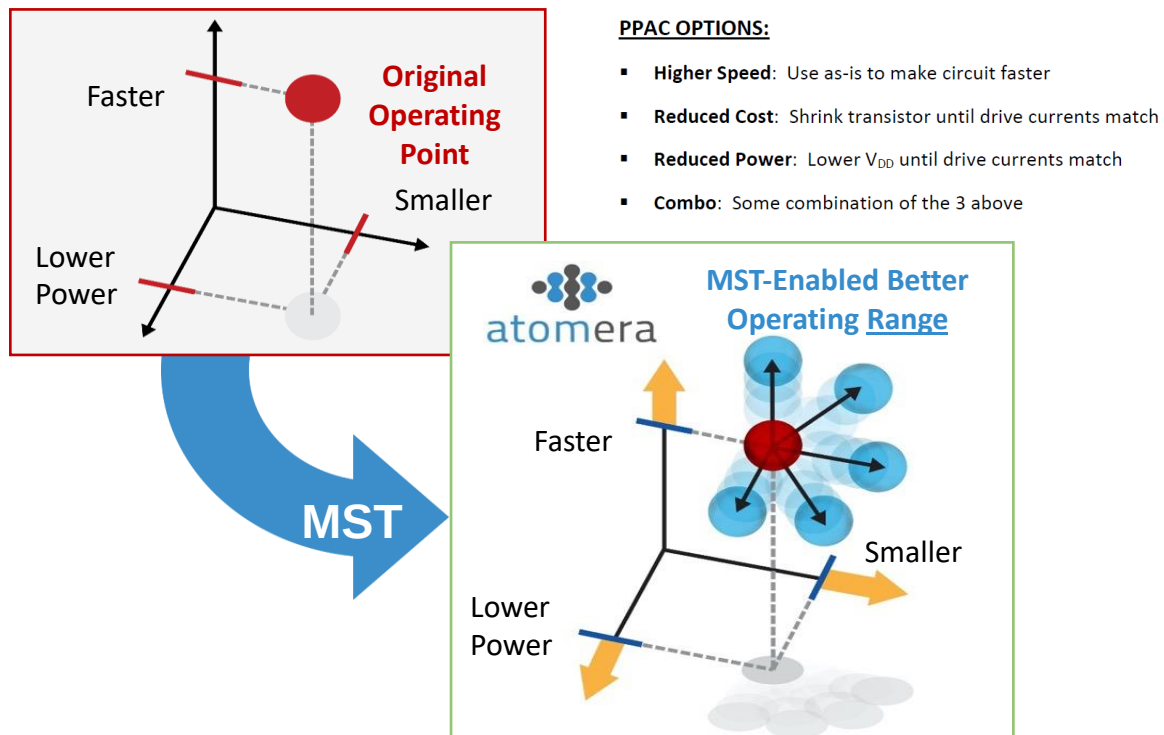


Figure 2: MST improves PPAC

Key Pain Points for GAA

The GAA manufacturing process is highly complex and many scaling challenges remain. The creation of stacked transistors requires selective growth of an epitaxial stack of silicon and silicon-germanium (SiGe) and subsequent removal of the sacrificial SiGe layers. The vertical stacking density is constrained by the need, later in the process, to insert HKMG layers between the individual stacked devices (called nanosheets or ribbons or bridges, depending on the manufacturer). The vertical stacking density thus depends on the thickness of the required HKMG layers. This is a key point we will return to later and was identified in a recent Intel presentation.

Nanoribbon Challenges

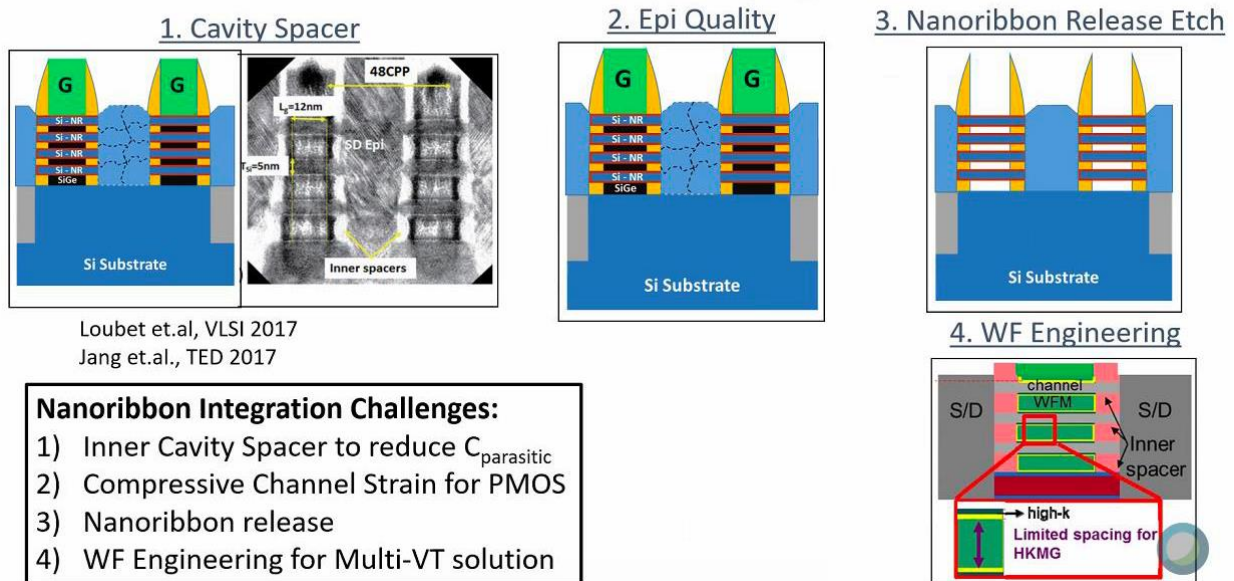


Figure 3. GAA (Nanoribbon) challenges from recent presentation by Tahir Ghani, Intel. Note multiple epi steps in GAA flow and see particularly issue 4.

As the device gate length has been reduced with successive technology generations, the proportional contribution of the source/drain and contacts to the overall resistance has increased. This additional resistance limits the useful on-current for a given device design and operating voltage. Reducing this additional series resistance can lead to significant performance improvement.

To reduce the resistance, in GAA devices, the source/drain doping is increased beyond what can be achieved by conventional implant / anneal steps, by etching out contact regions and then epitaxially depositing very highly-doped silicon or silicon-germanium regions. But the gate length is now so short that it is imperative to find a way to block the diffusion of these highly doped regions into the transistor channel itself, or again risk losing control of the transistor, leading to unacceptably high leakage power. This is a second active area of device research.

In the early days of FinFET research, devices were fabricated on silicon-on-insulator substrates so there was no leakage path below the FinFETs themselves. However, to keep the cost down, commercial FinFETs are manufactured on cheaper bulk silicon substrates. This leads to the requirement for heavily doped regions below the FinFET devices to prevent a key leakage mechanism called punch-through. Not surprisingly, this doping region is known as a punch-through stop layer, or PTS. However, the FinFETs themselves need uniform, controlled and lower doping, so it is important to prevent up-diffusion from the highly-doped PTS layer. GAA

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devices have evolved from FinFETs and are still manufactured on bulk substrates, so this constraint has remained, and is exacerbated by the use of even shorter gate lengths.

Lastly, there is also a need to make good metal contact to the GAA's heavily doped source/drain regions. The metallurgy of these metal-semiconductor contacts is receiving much attention.

MST Key Benefits for GAA

Improved PTS layer

As we have seen, for both FinFETs and GAA, there is a requirement for high doping below the stack to reduce punch-through leakage, but also for low doping in the FinFET/GAA region. MST has been proven to block the up-diffusion of the highly-doped PTS layers with a MST layer of less than 5nm thick. This application was discussed in our 2021 White Paper, "MST Dopant Blocking for Advanced 3D Applications."

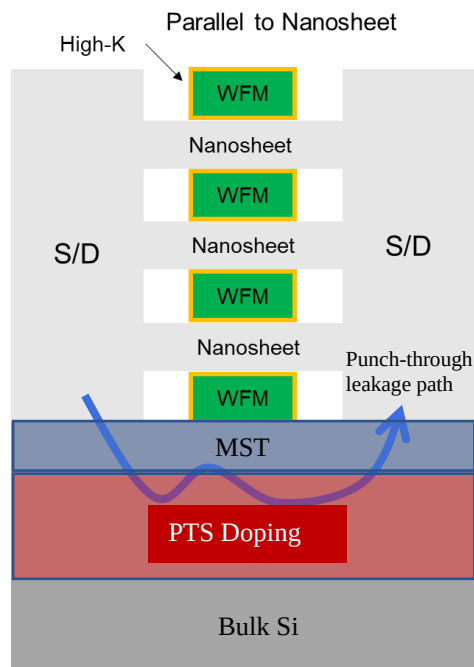


Figure 4(a) MST PTS Diffusion Blocker

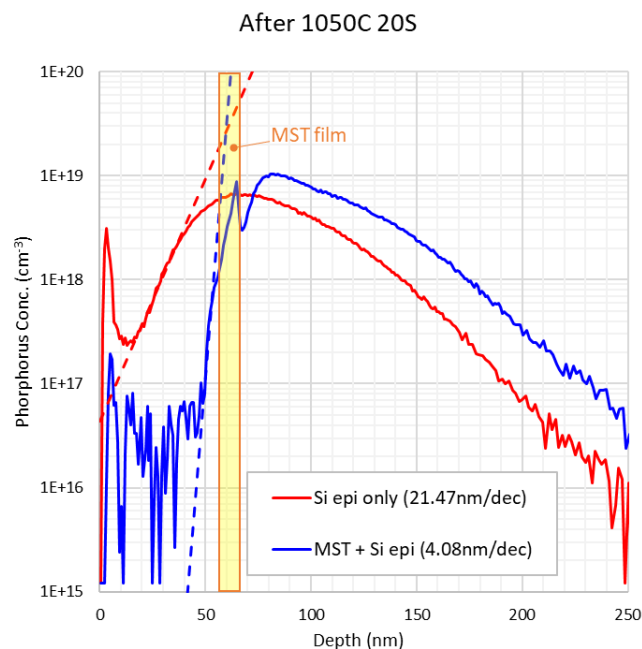


Figure 4(b) MST Phosphorus Diffusion blocking

In Figure 4(b) note that by suppressing diffusion mechanisms, MST enables higher Phosphorus doping in the PTS region as well as significantly reducing the up-diffusion into the silicon above the MST layers. This blocking can be achieved for Boron, Phosphorous and Arsenic for a total MST epi thickness of less than 5nm.

Improved High-Field Mobility from Reduced Surface Roughness Scattering

Over the past couple of years, Atomera has made good progress in characterizing the mobility improvement when MST is used in conjunction with HKMG gate-last technology as well as shedding further light on the origins of the mobility improvement under high vertical effective field (when gate voltage is high). For low effective fields, the mobility is dominated by Coulomb scattering from the charges introduced by doping. By reducing the surface doping, MST reduces Coulomb scattering, leading to significantly higher “peak” mobility, often as much as 50% higher. This operational mode (where the gate voltage is close to the device threshold voltage) is used in various analog applications and the MST benefit has been well characterized. However, for logic applications, the key is driving as much current as possible when the gate voltage is high. In this operational mode, the dopant charges are screened by the inversion charges, so that Coulomb scattering takes a back seat compared to phonon scattering (scattering from thermal vibrations of the silicon lattice) and surface roughness scattering.

Published research with the team from Notre Dame University[6], led by Prof. Suman Datta, confirmed MST mobility and gate leakage improvements in a planar gate-last HKMG process. (Prof. Suman Datta previously led the development of HKMG at Intel). Although the MST mobility improvement under high effective field was confirmed, the origins of the improvement need detailed characterization over a wider temperature range to distinguish between phonon scattering, which reduces as the temperature is decreased, and surface roughness scattering which is largely temperature independent, but is a strong function of the effective field.

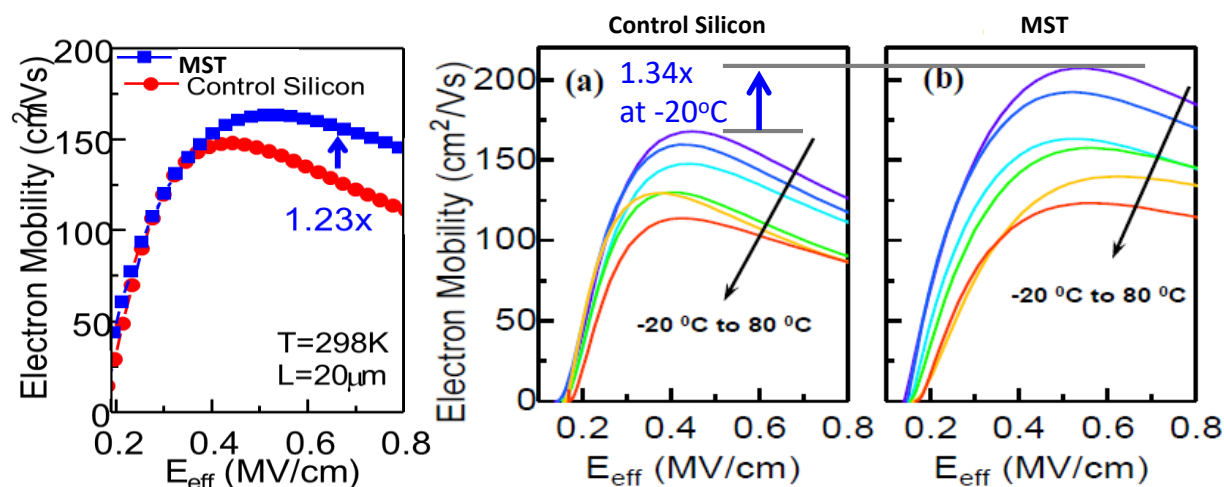


Figure 5. MST on gate last HKMG mobility characterization [6].

At lower temperatures, peak and high-field mobility increases as (thermal) phonon scattering decreases. The ratio of improvement for MST also increases because MST reduces surface roughness scattering.

Atomera is currently working with Professor Hiu-Yung Wong at San Jose State University to study MST mobility mechanisms across different temperature ranges. (Prof. Wong previously worked at Synopsys, and is an expert in device simulation and characterization.) In conjunction with the Atomera team, and thanks to a research grant from the National Science Foundation, Prof. Wong has made detailed over-temperature characterization of MST and control samples down to 4K (only four degrees above absolute zero, or -273C). At this temperature, phonon scattering is negligible, so that the high-field mobility is dominated by surface roughness scattering.

The results clearly demonstrate that the MST samples have >50% improved surface roughness scattering mobility compared to the control, and the details of these measurements have been submitted for journal publication. At normal operating temperatures, the higher phonon scattering restricts the MST benefit to 10-25%, depending on the effective field. Comparison with the room temperature measurements made with Notre Dame allows a detailed MST mobility model to be constructed. Under the typical operating conditions for nanosheets, the MST mobility advantage is expected to be about 15%.

While this improvement is significant, the channel mobility is only one factor in the overall current that can be driven. It turns out that there is another reason for introducing MST into the nanosheet channels (which can be done during growth of the Si/SiGe stack). Atomera discovered, working with Suman Datta's team, that MST improves the HKMG stack, as discussed in the next section.

Work Function (WF) Engineering

One of the most direct ways to increase density scaling is to reduce the vertical spacing between individual nanosheets (nanoribbons per Intel marketing). In addition to the high- κ dielectric, WF metal must be inserted to control the threshold voltage (V_t) of the individual nanosheets. High power, lower V_t devices need thicker metal, and this in turn limits the stacking density. WF metal research and reducing the metal thickness is thus a key area of R&D in GAA devices. We recently discovered that MST can reduce the interfacial dipole between the silicon channel and high- κ dielectric, thereby reducing the threshold voltage [4]. This is expected to enable higher GAA stacking density and is a key area of R&D at Atomera.

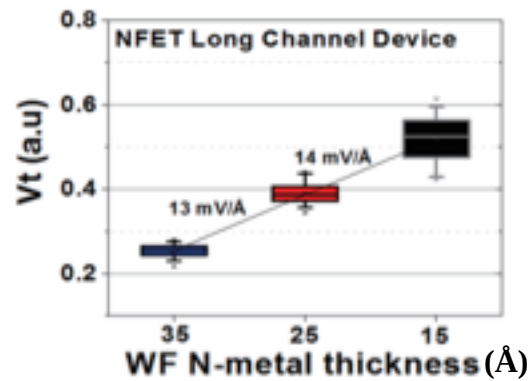
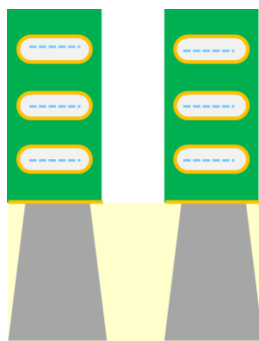


Figure 7. Low V_t requires thicker N-metal [7]

When high- κ dielectric is applied to silicon, an interfacial silicon oxide layer forms, with an associated charge dipole, since the oxygen has to be supplied from the covalent rare-earth oxide (e.g. Hafnium oxide). It is found that MST reduces this formation dipole, most likely because the MST oxygen layers can themselves supply additional oxide from within the silicon channel. Reducing the dipole leads in turn to a reduction in the effective work function, WF, leading to a lower threshold voltage, V_t , without having to increase the metal thickness. Furthermore, it is expected that WF can be tuned by varying the MST oxygen dose, providing a powerful tool for tuning V_t and increasing the vertical stacking density of nanosheets.

Single WF metal plus MST dose engineering for Multi- V_t

Thin WFM +
high oxygen
MST nanosheet
= low V_t



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low oxygen
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= high V_t

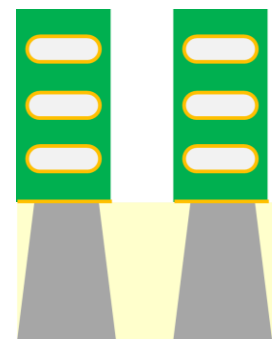


Figure 8. MST WF tuning by MST enables V_t tuning without requiring thicker WF metal stacks.

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Atomera is actively pursuing this new application for WF engineering. By using thin WF metal plus MST for tuning, more than a 10% increase in stacking density should be feasible compared to using thick metal.

Source/Drain Liner Diffusion Blocking

The combination of high source/drain doping to reduce series resistance, low nanosheet channel doping (to improve control and variability) and the relentless reduction of gate length puts an increasing constraint on the amount of permissible lateral diffusion from the epitaxially grown source/drain regions (eSD) into the channel. Too much diffusion and the off-state leakage becomes unacceptable. This diffusion issue has driven reduction in overall thermal processing budgets, but is constrained by epitaxial growth temperatures and the need to ensure activation of dopants. A source/drain liner of carbon-doped silicon has been traditionally used to reduce diffusion. MST offers an alternative dopant diffusion blocking technique that is far more effective. This MST layer can easily be grown epitaxially as part of the source/drain epi module.

An example using 2D MSTcad is shown below.

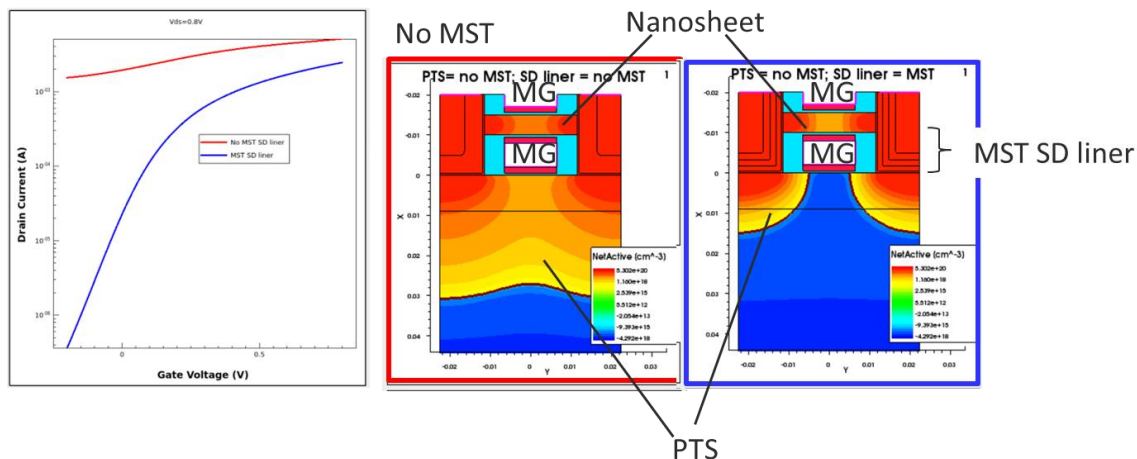


Figure 9. 2D MSTcad simulation of MST effectiveness as eSD liner after 1000°C spike RTA. Without MST eSD liner, Source and Drain are merged in PTS region due to diffusion of high concentration phosphorus. MST eSD liner can maintain separation of Source and Drain due to its diffusion blocking.

For the simulated conditions, MST reduces the off-state leakage by up to 10,000x Atomera believes that MST offers the most effective eSD liner option available.

Contact Engineering

As already discussed, the basic goal in logic design is to achieve the maximum current drive for a given supply voltage. In the planar era, the dominant source of resistance, and hence the limitation on the drive current, was the channel mobility. As nodes have scaled, the contribution of contact and series resistance have become more significant. In the section above, the MST liner maximizes the eSD retained active dopant retention and hence minimizes the eSD series resistance. But after the eSD deposition, the metal contact is also deposited and needs to have a low Schottky barrier height (SBH), to minimize the contact resistance. The various contributions to metal contact resistance are summarized below.

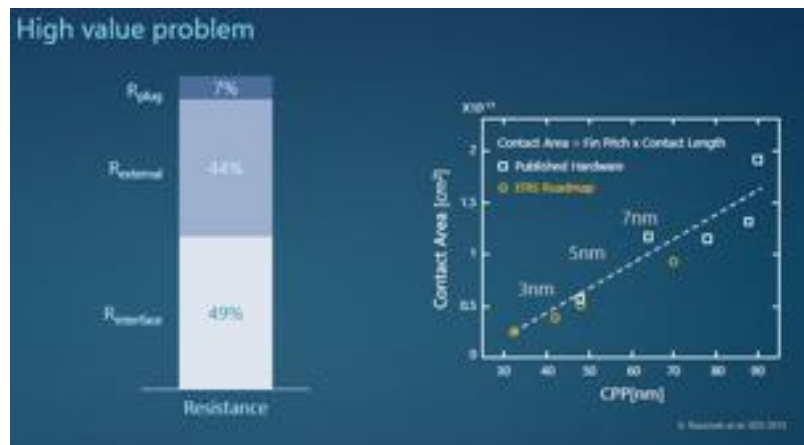


Figure 10. Contact resistance, including interface resistance from the Schottky barrier [AMAT MasterClass 2022]

Atomera-sponsored research at UC Berkeley led to a publication in AIP Advances 2020 [5], describing how MST can be used to engineer a lower Schottky barrier. The key result is shown below, for MST samples compared to control samples. Note that in the paper, MST is referred to as OI - oxygen insertion – to avoid use of the MST trademark.

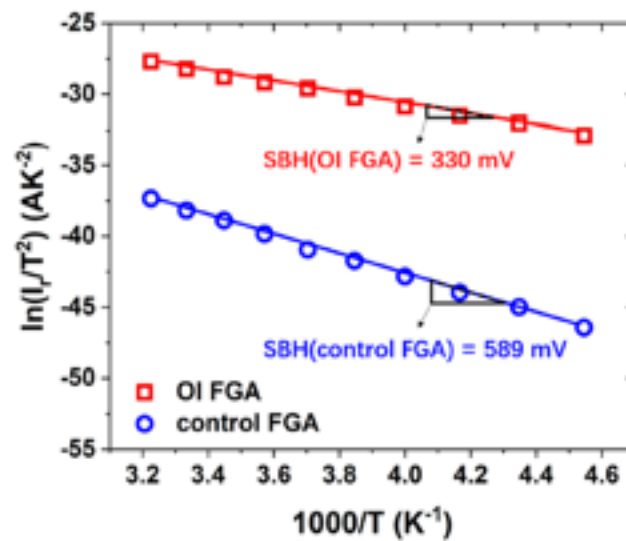


FIG. 6. Richardson plots for OI and control samples after FGA.

Figure 11 Richardson plot (from Figure 6 of [5]) showing reduction of SBH (given by slope of plot) for MST samples

The MST SBH reduction of 44%, from 589mV to 330mV, leads to a 22% projected reduction in contact resistivity and overall approximately 11% reduction in metal contact resistance.

Summary

MST has multiple applications in advanced GAA nanosheet devices. Si/SiGe epitaxy is already used in GAA fabrication to grow the Si/SiGe stack used for nanosheet formation, and in the contact plug for eSD.

MST can be used as a starting substrate (or as a blanket deposition early in the flow) for the formation of an effective PTS blocking layer. MST layers can be incorporated during the Si/SiGe stack growth module to provide a mobility boost and for WF engineering to improve vertical stacking density. MST can be included as the eSD liner in the early part of the eSD module. And finally, MST can be used just prior to metal contact deposition to lower the SBH and reduce metal contact resistance.

These benefits are additive and, if all used in conjunction, are projected to lead to multiple generations of GAA performance benefit.

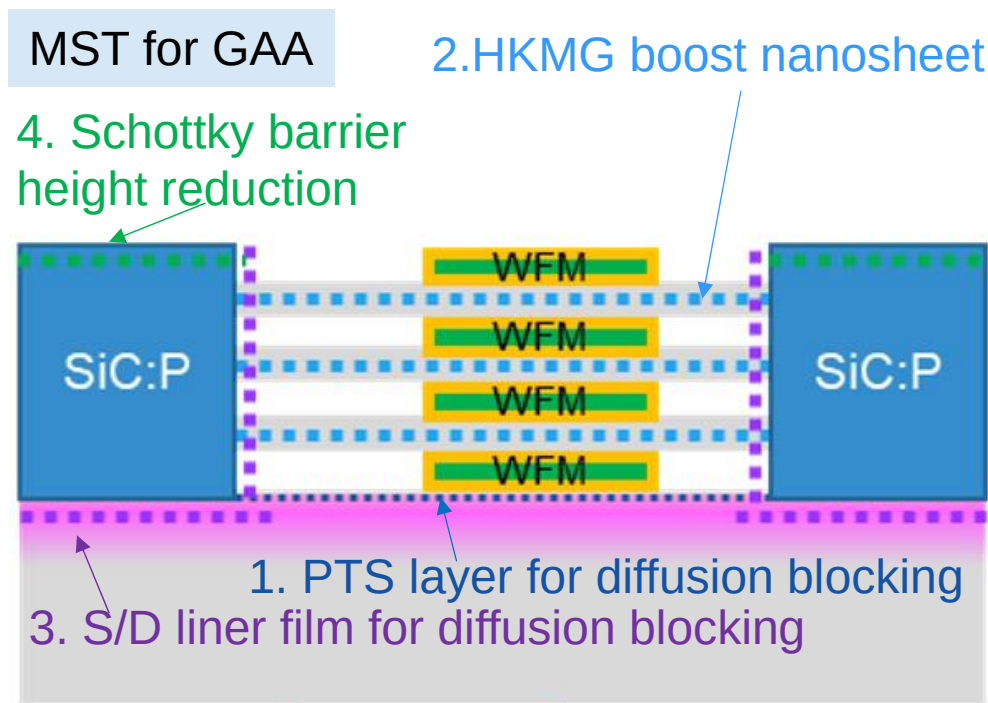


Figure 12 Summary of MST epi insertion points in GAA flow

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