

MST® for PMIC and RF-SOI Switches

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Outline

In this White Paper we first introduce Atomera's MST technology, and then take a brief look at the modeling of MST physics encapsulated in our Synopsys Sentaurus™ TCAD add-on, MSTcad™. We will then look at how MSTcad can be used to engineer an improved 5V switch for power management integrated circuit (PMIC) applications and improved RF silicon-on-insulator (RF-SOI) switches.

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Introduction

We call our technology MST, which stands for Mears Silicon Technology. MST is a “quantum-engineered” material to enhance transistor performance, based on over 15 years of R&D. Atomera is working closely with Synopsys to refine MSTcad, a TCAD add-on tool to the Synopsys Sentaurus™ suite of tools, which enables design and verification of semiconductor devices enhanced by MST.

So, what is MST? MST is a material typically built by inserting partial monolayers of oxygen into silicon, during silicon epitaxy, and we've developed recipes for all the major EPI tools that are typically found in major fabs. MST works across a wide technology space, from legacy planar nodes to the most advanced 3D applications. In essence MST gives you more drive current from

the same device footprint. Compared to a non-MST, or baseline device, MST provides improved PPAC - power-performance-area/cost.

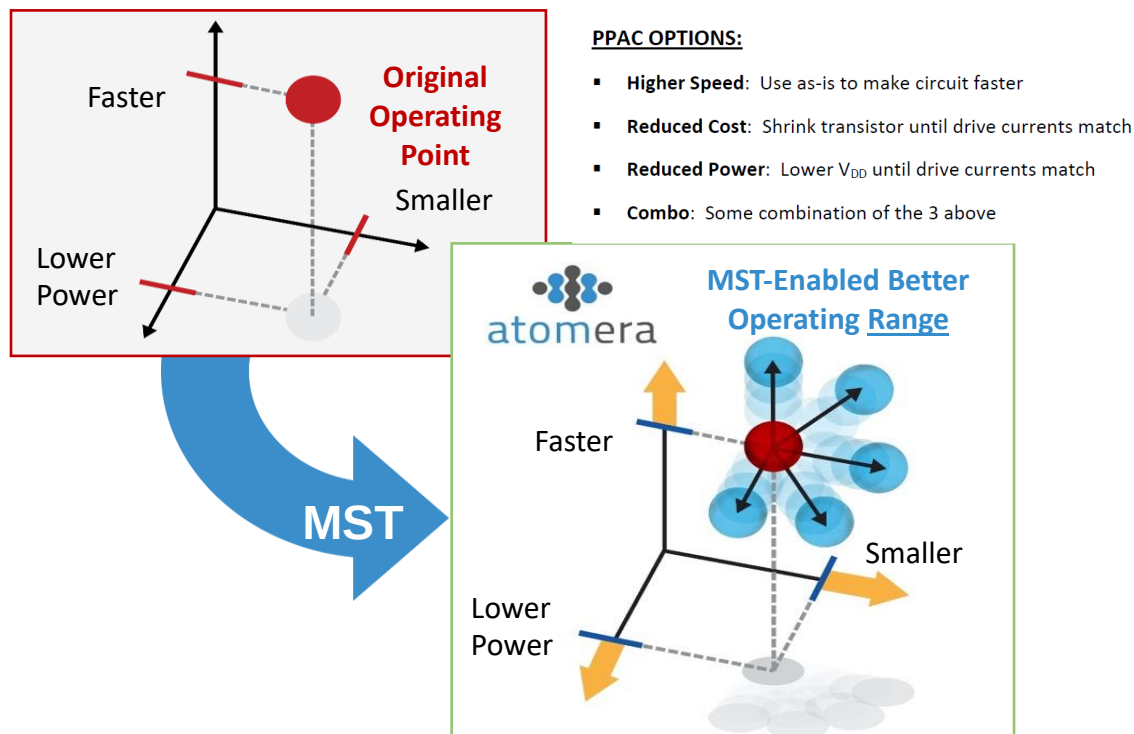


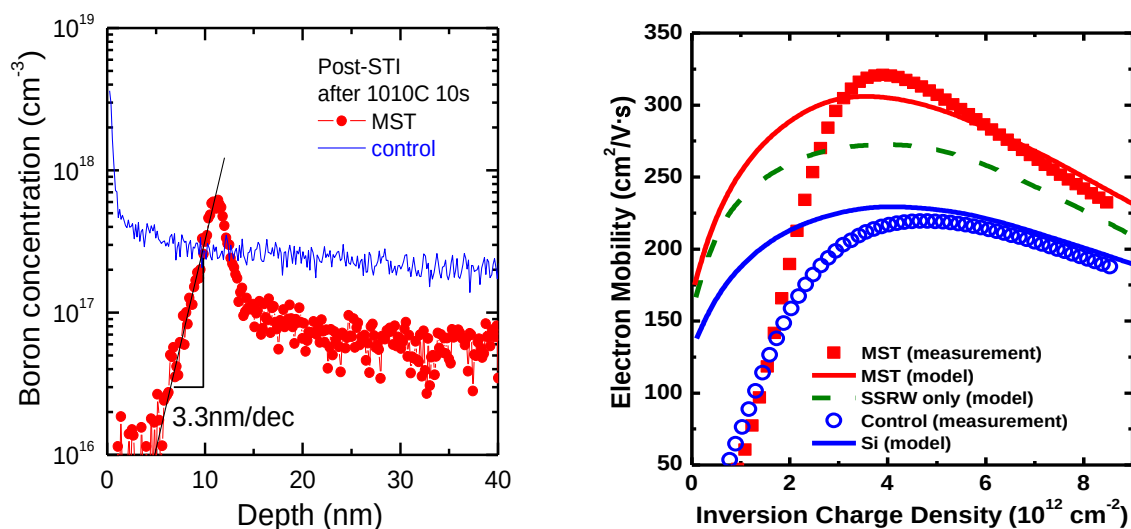
Figure 1: MST improves PPAC

An existing semiconductor device will have a baseline operating point that is a compromise of speed, cost and power. Depending on the sector and customer, we will typically trade off the various benefits of MST technology to provide higher speed or reduced area and hence cost or reduced power, or some combination of all three!

MST Toolbox for Improved CMOS

MST can be thought of as a toolbox for improving both NMOS and PMOS devices. Perhaps the most significant aspect of the technology is its ability to engineer doping profiles with far more abrupt transitions than could otherwise be obtained. An example is shown on the left of Figure 2. Delta-doped and super-steep retrograde profiles are well-known to improve short channel effects, enabling better device scaling. Also, by keeping the dopants away from the dielectric interface, we can significantly reduce random dopant fluctuation, leading to reduced variability and mismatch.

MST also provides fundamental mobility enhancement for both electrons and holes. Higher current at the same V_t is another part of the MST improvement in PPAC. Other MST benefits we've measured are reduction in gate leakage and improved gate dielectric integrity for nitride and High-k dielectrics, leading to improvement in reliability metrics such as TDDB and NBTI.



❖ N. Xu et al., APL¹⁰⁷, p.123502 (2015)

Figure 2. Key benefits of MST: dopant engineering and mobility enhancement

MST Key Benefits Across Nodes

MST is applicable across a very wide technology space. Figure 3 shows the relative contributions of dopant engineering, mobility and reliability engineering, based on the combination of a variety of electrical device data and device modeling.

We've found that the dopant engineering capability offered by MST enables us to engineer improved devices across most of the semiconductor technology space. In this paper, we are focusing on engineering a 5V device for PMIC applications and an RF-SOI switch. We chose this particular device because it has been highly optimized by many engineering teams over the years and further undiscovered improvements are particularly hard to find.

While there is always some mobility benefit from MST, part of the mobility benefit comes from reducing the degradation caused by high doping adjacent to the dielectric interface. Since many analog devices use low channel doping, in this application MST is used less for a mobility benefit but is more focused on dopant engineering.

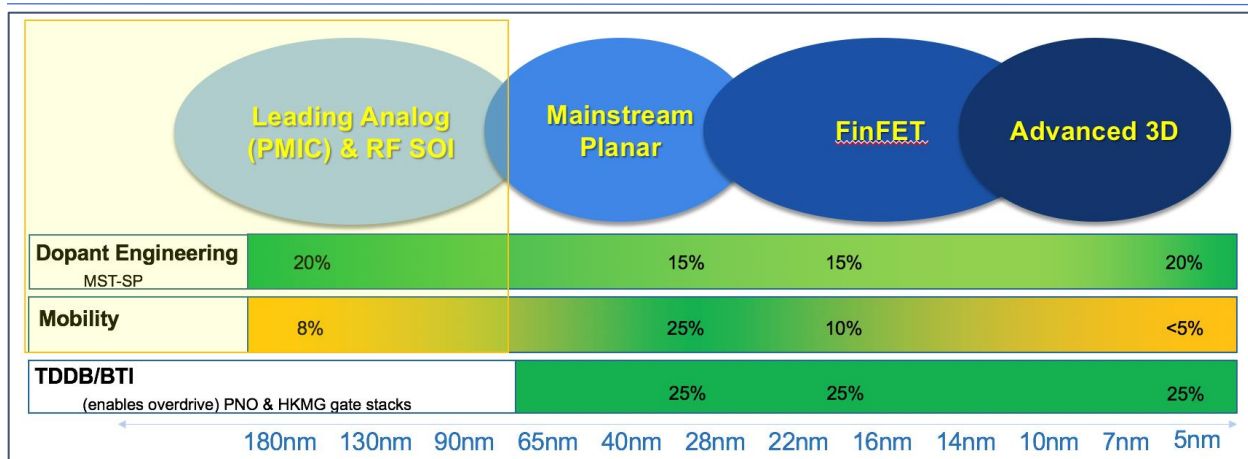


Figure 3. Key benefits of MST across different nodes. Highlight shows focus for PMIC and RF-SOI

MST Structure — Oxygen in Silicon Lattice

To help us understand the origin of the MST benefits, we need to start with the interaction of the MST oxygen atoms with the silicon lattice. Figure 4 shows an idealized structure of an MST oxygen layer.

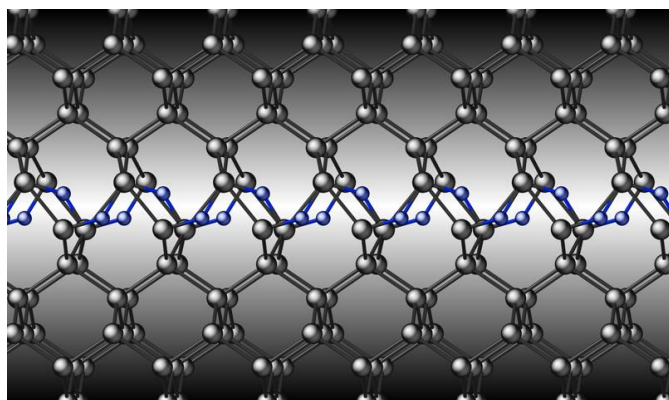


Figure 4. Idealized structure of an MST oxygen inserted layer

In general, MST is a class of artificial, metastable structures that are self-stabilized by the interaction of the oxygen atoms via the silicon lattice. Actually, MST isn't restricted to silicon and oxygen, but it is simpler for this illustration. We say metastable, because the lowest energy configuration for silicon and oxygen atoms is silica — SiO_2 , where each silicon is bonded to four oxygens. Fortunately, there is an energetic barrier to the formation of silica, and so MST has a high thermal stability. The oxygen in these MST structures is interstitial rather than substitutional, with each covalently bonded to two adjacent silicon atoms. You can see that there is some local

distortion of the silicon lattice to accommodate the oxygen. This distortion becomes negligible once you are about four silicon layer spacings away from the oxygen.

While a single interstitial oxygen diffuses quite freely in silicon, in MST the adjacent oxygens have a “collective” self-stabilization mechanism so that overall, the MST oxygens find a lower energy minimum when they are both proximate to a silicon. As a result, the MST oxygen is much more thermally stable, and this is the key to the successful integration into a variety of semiconductor manufacturing processes. Over the years of manufacturing MST films, we have also found recipes that improve the thermal stability. As a rough guide, the current limit on a thermal Dt is approximately 1100C for 60s for the highest thermal performing MST films, and the anneal ambient (oxidizing or inert) also affects the oxygen stability. As we shall see, in modelling MST, the key interactions that concern us are the interaction of oxygen atoms with the silicon lattice and the mutual interaction with electrical dopants and point defects.

MST Dopant Trapping & Diffusion Blocking

MST provides an unprecedented ability to engineer the doping profile throughout a typical semiconductor manufacturing process. There are two key mechanisms. Because of the local lattice distortion and electronegativity of the oxygen, electrical dopants are trapped close to the MST oxygen layers. This results in the formation of a sharp dopant peak, which can be positioned by design of the MST layers. The trapping is shown in Figure 5, for MST oxygen layers at a depth of around 15nm, for boron, phosphorus and arsenic.

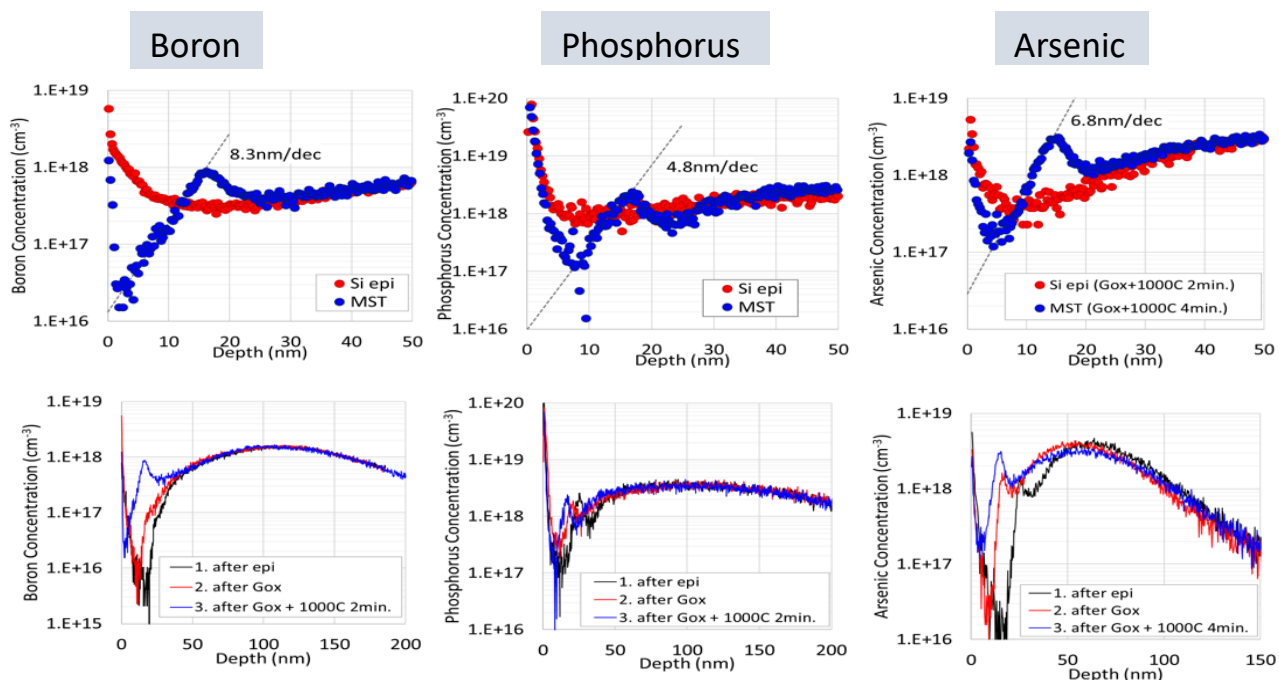


Figure 5. Dopant trapping and diffusion blocking with MST for boron, phosphorus and arsenic

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Not only is dopant trapped, but further up-diffusion is in effect retarded, so that a super-steep retrograde profile is formed. These profiles are well-known to reduce short-channel effects and reduce variability from random dopant fluctuation. It is important that these profiles are retained even after formation of thick gate oxides and typical activation anneals.

The second mechanism is more subtle but has many applications. As can be seen in the lower part of the figure, which is taken on a greater depth scale, we have found that the as-implanted dopant peak sees much less diffusion than would be expected from oxidizing anneals.

This is because the MST oxygen also traps, and hence, blocks silicon self-interstitials. The interstitial flux during gate oxidation is well-known to cause significant diffusion of as-implanted dopants. By blocking this flux, MST allows precise, stable positioning of implants, which do not significantly diffuse, vertically OR laterally, during subsequent anneals. This is the key to engineering precise junctions and other dopant profiles.

MSTcad Overview

For the past few years, Atomera has been working closely with Synopsys to develop an add-on capability to the Synopsys Sentaurus™ suite of TCAD tools, for modeling MST. MSTcad uses the Alagator scripting language supported by Sentaurus.

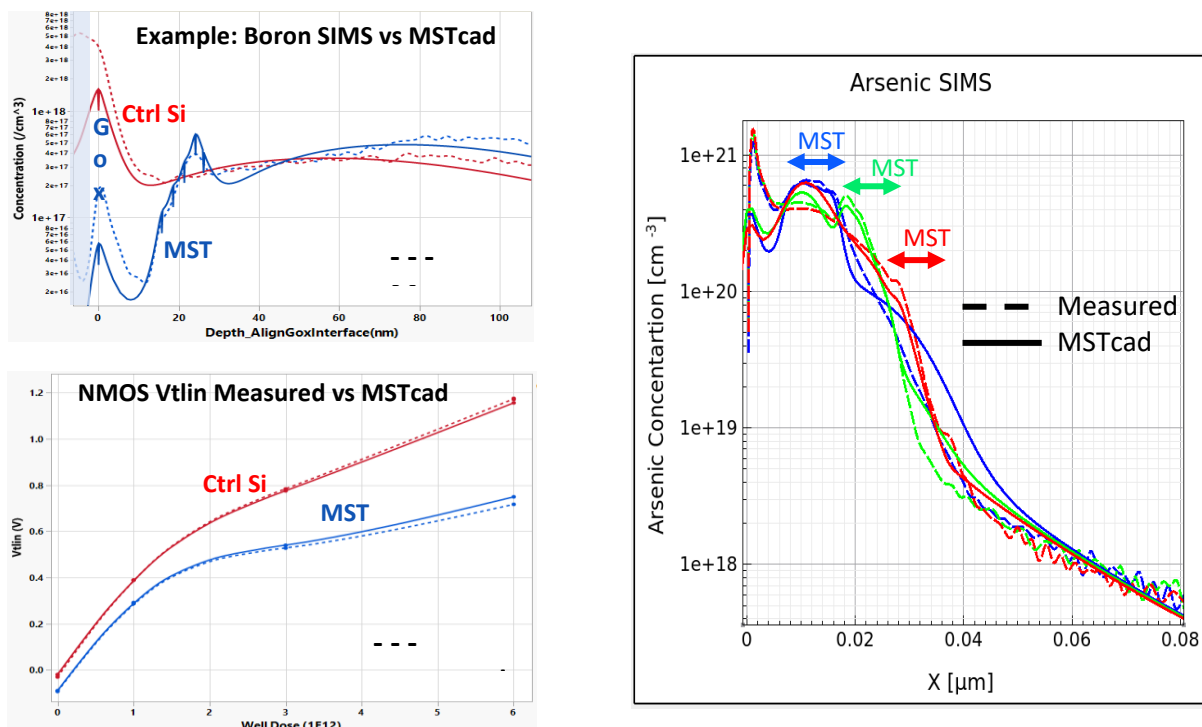


Figure 6. MSTcad™ comparison with physical SIMS and electrically measured Vtlin

The unique doping profiles enabled by MST are well-captured in the upper left of Figure 6 compared to physical SIMS (Secondary Ion Mass Spectroscopy). The doping profiles integrate into S-Device so that electrical parametrics can be simulated. As an example, in the lower left figure, the V_t dependence on well dose is also closely modelled.

Atomera published a paper in 2020 with authors from UC Berkeley showing that MST can also be used to retain shallow junctions because of dopant trapping. In the paper, we were able to show a 30% reduction in junction depth without increasing series resistance for boron, phosphorus and arsenic. As can be seen on the right side of Figure 6, even for arsenic levels in the mid E20s, MSTcad lines up very well with the experimental data. In addition to working with customers, Atomera uses MSTcad internally to develop new silicon products, such as MST-SP and improved RF-SOI switches.

Engineering Improved 5V Power Devices for PMIC: MST-SP

We recently launched our MST-SP product, an asymmetric 5V power device for PMIC and other applications. MSTcad has played a crucial role in the optimization of MST-SP.

MST itself helps the design and scaling of 5V devices because of two features. The inherent mobility enhancement provides higher I_{dlin} and hence lower on-resistance. But the precise doping control and diffusion retardation enabled by MST further helps breakdown voltage and device scaling, giving an overall significant reduction in specific on-resistance, R_{sp} for the same breakdown voltage.

MSTcad Optimization of MST-SP

We have been able to verify MSTcad™ and the MST-SP design on multiple silicon lots run at our partner TSI Automotive-qualified Foundry in Roseville, CA.

We have established very good alignment between silicon data and MSTcad simulation over a variety of electrical characteristics, including reliability parameters such as HCI and TLP-SOA, as shown in Figure 7.

Lg Param	0.26			0.28			0.40		
	Meas	TCAD	%Δ	Meas	TCAD	%Δ	Meas	TCAD	%Δ
Vtgm	0.90	0.88	-2.8%	0.93	0.92	-1.0%	0.99	0.91	-7.8%
Rsp	0.74	0.76	2.4%	0.79	0.81	2.1%	1.16	1.17	0.7%
BVDSS	10.8	10.6	-1.9%	11.2	10.8	-3.9%	12.6	11.2	-11.3%

Figure 7. Comparison of measured DC parametrics with MSTcad™

Now that we have a silicon verified MSTcad tool, we can use it to optimize the implants of the asymmetric MST-SP device. Of course, the optimization is multi-dimensional, with many device

care-about including reliability parameters as well as Idlin (Rsp) and BV. MSTcad™ and Sentaurus™ allow sophisticated response surface characterization as individual implants are varied.

The baseline process symmetric device has a gate length of 0.7um. By adopting the asymmetric MST-SP design, we were immediately able to scale to a gate length below 0.4um. However, thanks to the detailed optimization enabled by MSTcad, we have successfully scaled the design to a gate length of 0.25um, while meeting reliability for a DC-DC converter.

The result is a robust 5V switch with industry-leading parametrics, as shown in Figure 8. To our knowledge, the Rsp-BV for the engineered 0.25um devices is the best in the industry for an automotive-qualified 180nm process. The beauty of the design is that it offers a straightforward path to implementation on smaller geometry processes, and thanks to the tighter design rules, the Rsp is projected to be even further reduced, using essentially the same doping design between source and drain.

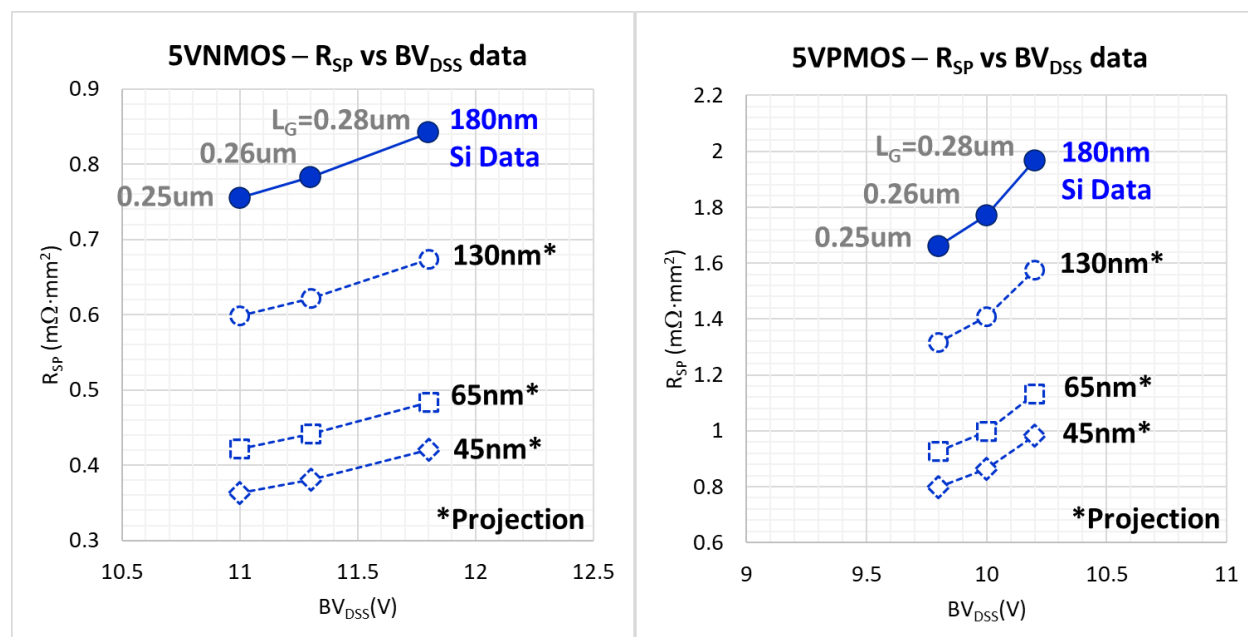


Figure 8. MST enables “best-in-class” 5V power switch performance. Note that data have been updated reflecting device improvement after publication in IEEE ISPSD 2022

MST Improved RF-SOI

It has long been known that placing a highly doped “ground plane” region close to the buried oxide (BOX) of a silicon-on-insulator device would improve the gate length scaling. For example, in a paper in 2005, authors from IBM proposed and demonstrated such a device at the International Electron Devices Meeting (IEDM), as shown in Figure 9.

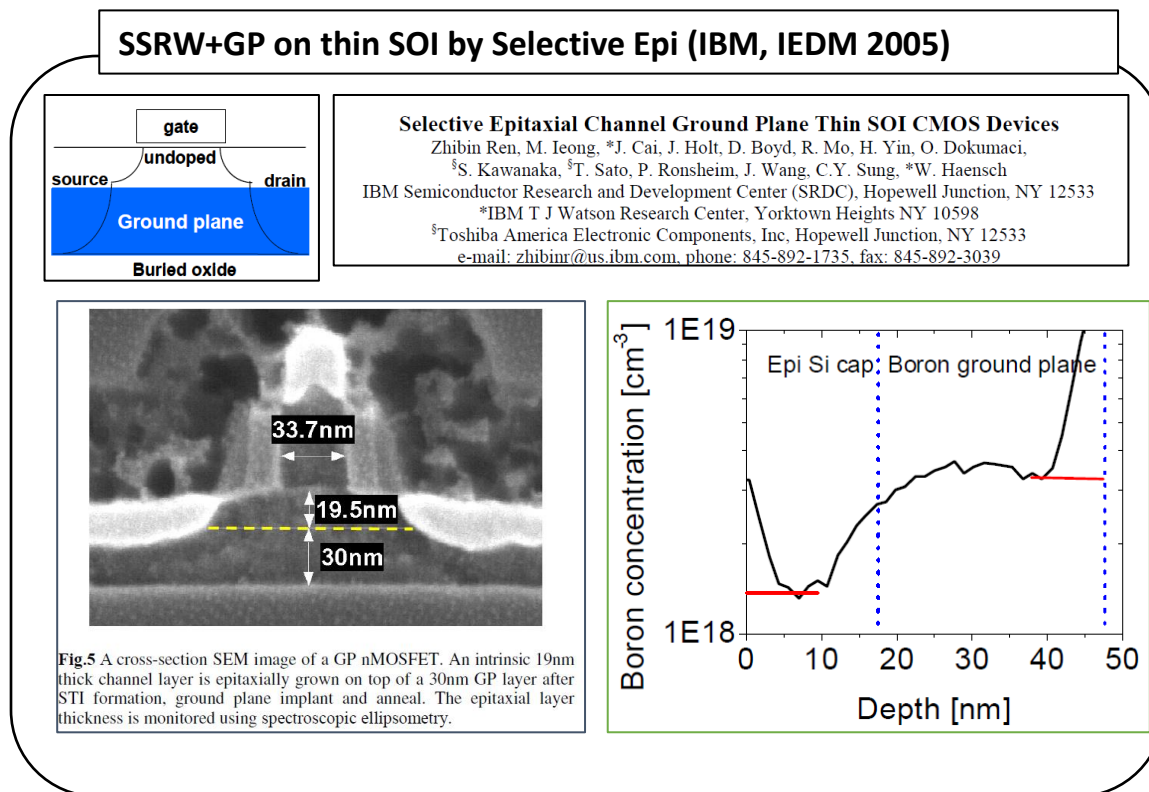


Figure 9. Ground plane thin SOI device as published by IBM (IEDM 2005)

In order to create such a structure, the authors from IBM deposited undoped epitaxial silicon on a boron-doped SOI structure by selective growth and then used a highly restrictive low thermal Dt process to reduce up-diffusion of the boron. Even so, they were only able to achieve about a factor of two difference in boron doping in the surface compared to the region close to the BOX.

As we have seen, MST can prevent up-diffusion of boron, even for normal semiconductor thermal processing, and the dopant trapping by the MST oxygen layers, enables a much higher ratio of doping between the “ground plane” and the surface region.

Using wafers from Soitec, Atomera has been able to demonstrate the unique dopant retention of MST on ultra-thinned RF-SOI substrates. Regular RF-SOI (high resistivity, trap-rich) substrates were thinned to 120Å silicon on BOX thickness, and then blanket MST layers plus a 30nm capping silicon layer were grown. After growth, and during regular device fabrication, the wafers were implanted with boron. The as-implanted boron profile is quite broad as shown in the white open circles in Figure 10. The MST oxygen layers then trap diffusing boron to create the steep profiles as shown in blue (after RTA anneal) and red (after full thermal Dt of the RF-SOI manufacturing process). Compared to the SSRW profile formed by selective epitaxial growth on the boron-doped

SOI structure in Figure 9, MST enables greater than a10x steeper SSRW profile by implanting boron into the SOI substrate after blanket MST epi growth.

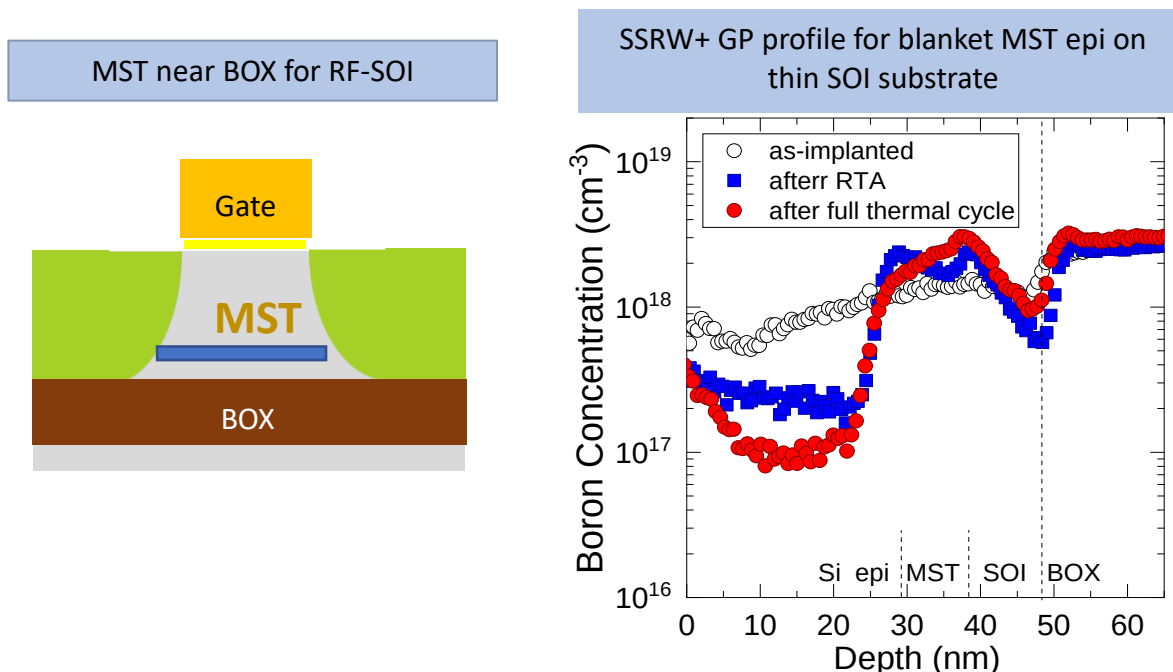


Figure 10. MST provides boron retention and steep retrograde channel profile in RF-SOI

One of the key constraints in scaling these switches to improve $R_{on} \cdot C_{off}$ is that we lose breakdown voltage for shorter gate length, thinner SOI devices. By positioning MST dopant trapping layers close to the buried oxide, we have been able to provide a conductive path to the body contact at the edge of the switch, enabling further device scaling without compromising the breakdown voltage.

MSTcad Verification of RF-SOI

Atomera has now verified that the doping profiles seen in the experimental data of Figure 10 can be simulated using MSTcad. Silicon lots at the TSI foundry have been used to compare physical SIMS with MSTcad, as shown in Figure 11.

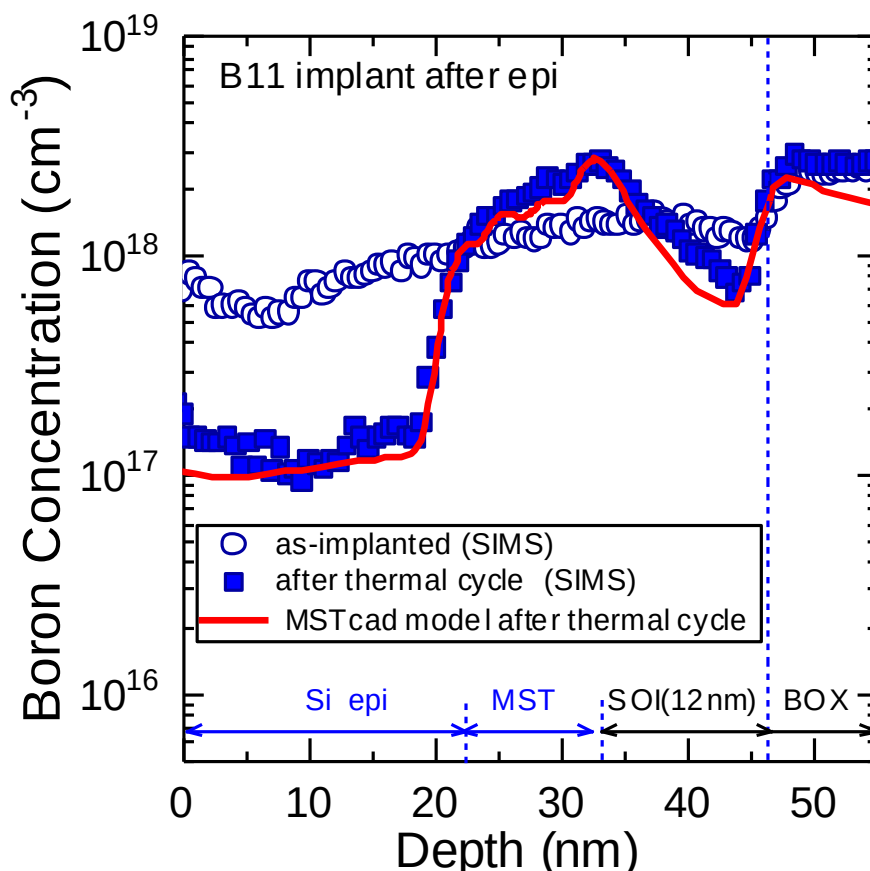


Figure 11. Verification of MSTcad model for RF-SOI compared to physical SIMS for silicon lots runs at TSI Foundry. Further electrical lots are in process.

3D Simulation of RF-SOI

Since the breakdown mechanism impeding the scaling of RF-SOI switches arises from accumulation of generated holes, and the associated rise in potential near the middle of the wide switch devices, it is important to verify the MST advantage using 3D TCAD simulation.

Atomera is fortunate to work with Prof. Hiu-Yung Wong, formerly of Synopsys, and now a professor at San Jose State University. With the help of Prof. Wong, we have been able to simulate a full switch device in 3D, with the addition of ground plane doping near the BOX, as facilitated by MST. The simulation result is shown in Figure 12. Devices of various gate lengths and overall thickness of silicon-on-BOX were simulated and the $R_{on} \cdot C_{off}$ evaluated for acceptable breakdown voltage.

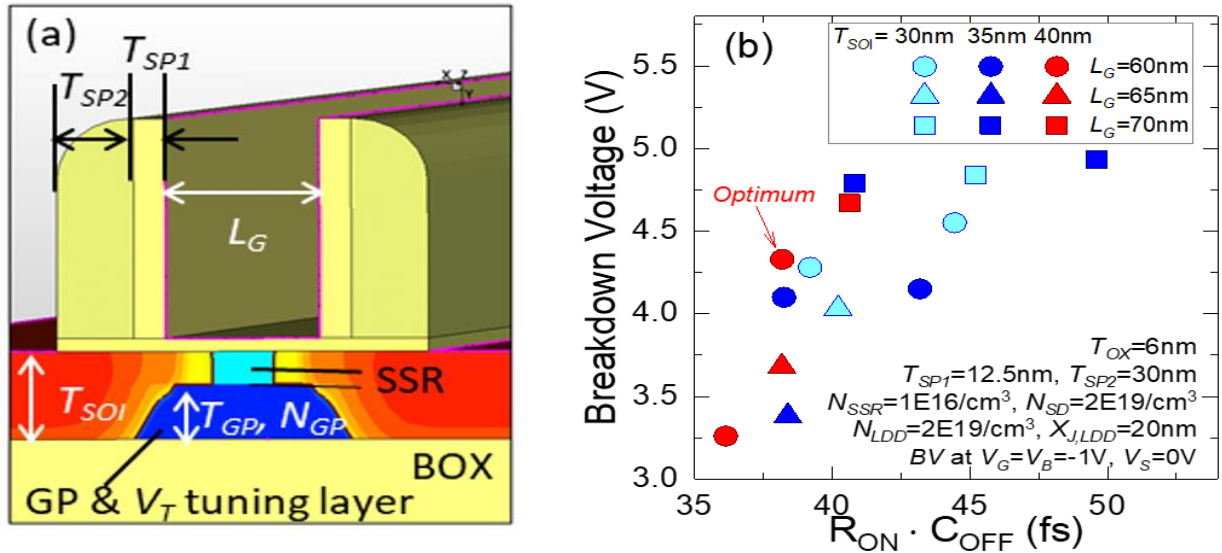


Figure 12. 3D TCAD simulation of breakdown voltage vs. $R_{on} \cdot C_{off}$ for MST ground-plane devices

It is found that $R_{on} \cdot C_{off}$ below 40fs is achievable with the MST ground plane doping, compared to current state of the art for RF-SOI around 90fs. Electrical verification is in process.

Summary

MST provides doping engineering and mobility enhancement, enabling the further scaling of key semiconductor switch devices. MSTcad is a silicon verified tool for Sentaurus users, which helps optimize the integration of MST. We have used MSTcad to engineer MST-SP, an industry-leading 5V switch for PMIC applications. MSTcad is actively in use to improve higher voltage and RF-SOI devices, and there are many further applications of the technology.