

MST® Breakthrough for RF GaN on Silicon

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Outline

Gallium nitride (GaN) has emerged as a leading semiconductor material for power and RF devices [1], driven by its superior high-frequency performance and strong figures of merit compared with silicon, silicon germanium, and gallium arsenide. GaN can be grown on several substrate platforms, including sapphire, silicon carbide (SiC), and silicon. Among these, silicon offers the advantages of lower cost, larger wafer availability, greater manufacturing scalability, and potential for CMOS hetero integration. Although GaN-on-silicon (GaN/Si) power devices have gained meaningful commercial traction, RF GaN/Si has not achieved the same level of market adoption as GaN-on-SiC, largely due to higher RF losses.

Over the past two years, Atomera has been working to improve GaN/Si material quality and device performance. This white paper presents recent findings on Atomera's MST® technology and its potential to enhance GaN/Si devices. In collaboration with our partners, we have demonstrated improvements in crystal quality and reduced leakage in lateral high-electron-mobility transistors, or HEMTs. These improvements support higher-voltage operation and improved device performance.

For RF applications, GaN/Si frequency response has been limited by the parasitic channel that forms at the interface between the GaN epitaxial layer stack, typically initiated with an aluminum nitride (AlN) nucleation layer, and the silicon substrate. This parasitic channel is a major source of excess RF loss compared with GaN-on-SiC and other established RF technologies, such as RF SOI. Recent data show that inserting a thin MST layer before growth of the GaN stack can reduce parasitic charge by more than an order of magnitude. This reduction can substantially lower RF losses while improving linearity and power handling, helping to close the performance gap between GaN/Si and higher-cost RF substrate platforms.

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Introduction

We call our technology MST, which stands for Mears Silicon Technology. MST is “quantum-engineered” to enhance transistor performance, based on over 20 years of R&D. In our previous white papers [see e.g. 2,3], we focused on the proven ability of MST to engineer doping profiles and reduce dopant diffusion, thus enhancing a broad swathe of silicon devices from power switches to leading edge gate all-around (GAA) devices.

In this paper we focus on a different aspect of MST, enabling improvements in heteroepitaxy, or in other words the growth of other semiconductor materials on silicon. We have found that adding a thin layer of MST to a silicon substrate prior to growth of a typical gallium nitride (GaN) stack can result in multiple benefits, particularly for RF applications. We believe that the benefits are game-changing, paving the way for GaN-on-silicon to enter the mainstream of RF applications in 5G & future 6G networks.

GaN-on-silicon basics

Silicon has huge advantages as a starting substrate in terms of cost and scalability. Silicon’s crystal lattice structure is not matched to that of GaN, however, resulting in dislocations in the transition region between the two materials which extend upward into the active GaN layer. These dislocations can substantially degrade device performance. The dislocation density generally reduces as more material is grown. For a 650V GaN power device, the GaN thickness typically needs to be of the order of 4-5 μ m, which is relatively thick so it can mitigate some dislocation density. RF GaN is typically thinner, on the order of 2 μ m, so dislocations are more prevalent.

Furthermore, the different semiconductor materials have different thermal expansion coefficients, meaning that when the wafer is cooled back to room temperature from the growth temperature of around 1000C, the wafer can bow or warp. An illustration of this issue, taken from a white paper by Okmetic [4], a leading supplier of engineered substrates for GaN-on-silicon and other RF technologies, is shown in Fig. 1. MST® for RF GaN-on-Si.

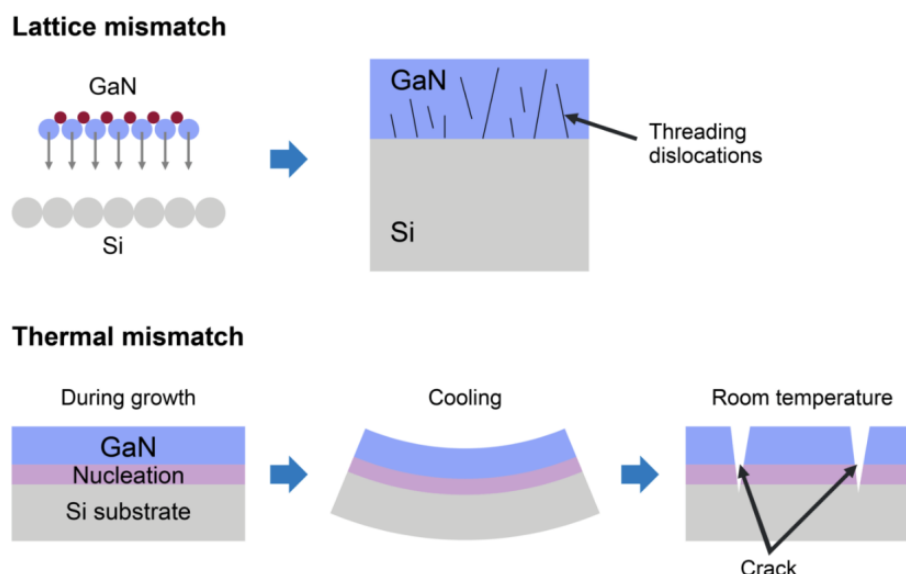


Fig. 1 The lattice mismatch and thermal mismatch issues for GaN-on-Si [4].

For this reason, multiple layers of different composition are grown prior to the GaN growth. The first of these layers, known as the nucleation layer, is typically aluminum nitride (AlN). A typical GaN stack for RF applications is shown in Fig. 2. As you can imagine, there has been a huge engineering effort to understand and reduce dislocations as well as to control wafer bow. The good news is that this engineering effort has reached a level of maturity where GaN/Si for power is economically viable and its superior technical benefits have enabled GaN power devices to be a strongly growing market. Yole are predicting a 40% CAGR for the GaN power market over the next five years [1]. One of the first commercial applications is in rapid charging, where the superior characteristics of GaN enables higher efficiency switched-mode power supplies, such as DC-DC converters for cell phones.

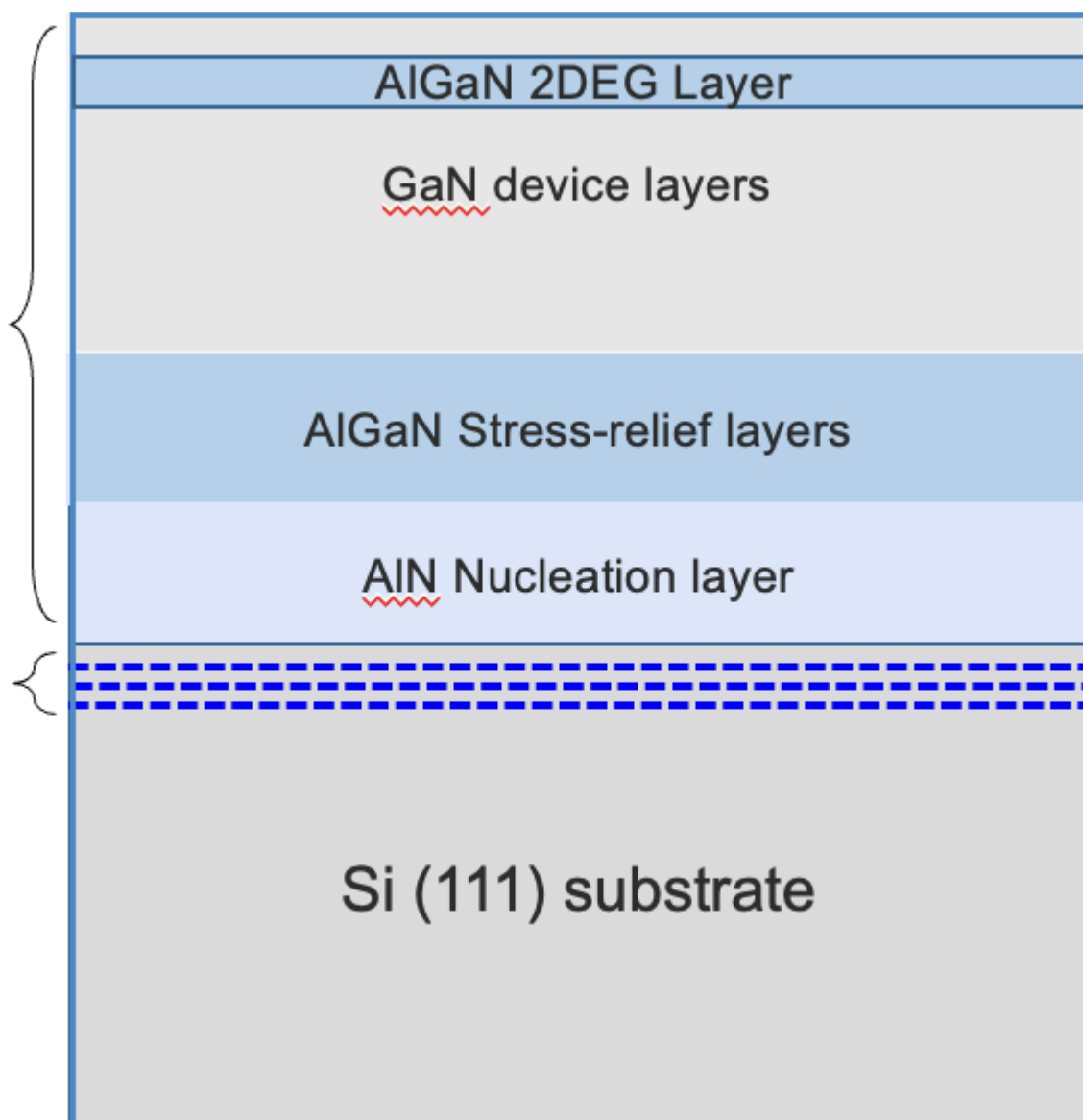


Figure 2. Schematic of RF GaN-on-Si wafer and location of MST at surface of Si (111) substrate.

GaN-on-silicon's RF problem: the parasitic channel

A primary reason that RF applications have lagged power applications for GaN is the formation of a parasitic charge layer that forms at the silicon interface, which leads to excess RF losses and poorer linearity and power handling compared to other technologies. Incorporation of Al or Ga, which act as p-type dopants in silicon during fabrication, creates the unwanted parasitic charge layer. During the formation of the nucleation layer and subsequent processing of the wafer, a layer of charge is incorporated at the interface, even when the starting silicon substrate itself is very high resistivity. A schematic of the formation of this parasitic channel is shown in Fig. 3.

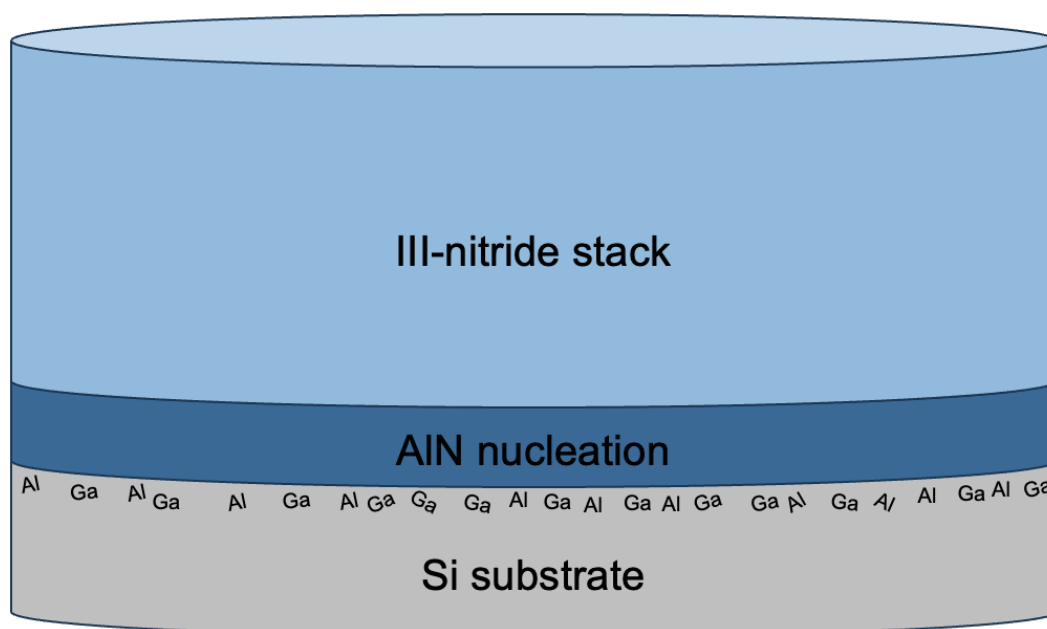


Figure 3: Schematic of formation of parasitic channel at interface of silicon substrate and first layer of the GaN stack (aluminum nitride).

Atomera and GaN-on-silicon

Recently, Atomera initiated a program to demonstrate the benefits of MST for GaN-on-silicon. Atomera already believed that MST would bring advantages to heteroepitaxy [5], and judged that it was timely to bring a new performance-boosting technology to the GaN/Si market. Atomera is working with well-known GaN industry experts including Wayne Johnson of Soundside Partners and Prof. Edwin Piner's group at Texas State University.

RF GaN stack growth for Atomera

The Texas State group has a well-established high-performance RF GaN baseline stack similar to that shown in Fig. 2 [6,7]. The stack starts with an AlN nucleation layer for which the MOCVD process has been carefully optimized to incorporate the latest "nitridation" learning to help reduce the parasitic channel [8]. Stress-

relieving AlGaN layers are then grown, followed by the GaN buffer and the active 2D electron gas (2DEG) layer used for the high electron mobility transistor (HEMT).

Crystal quality of the AlN and GaN layers is monitored using X-ray diffraction (XRD). Typically, both the [0002] symmetric and [0014] asymmetric XRD signals are tracked to provide insight into different types of dislocations in the film. The Texas State baseline has a stable GaN [0002] XRD full-width half maximum (FWHM) of 650+/- 10 arcsec, a very good value for a film of this thickness.

MST layers of various structural compositions were grown on starting silicon (111) substrates and then shipped to Texas State for growth of their baseline GaN stack. Various reference GaN/Si wafers were also grown to monitor the stability of the baseline.

Not all the MST recipes improved the crystal quality, but this first screening exercise identified clear directions for the MST growth. The best-performing MST recipe exhibited more than 20% improvement in the GaN crystal quality, as measured by XRD. The plots of the reference wafer and MST wafer are shown in Fig. 4.

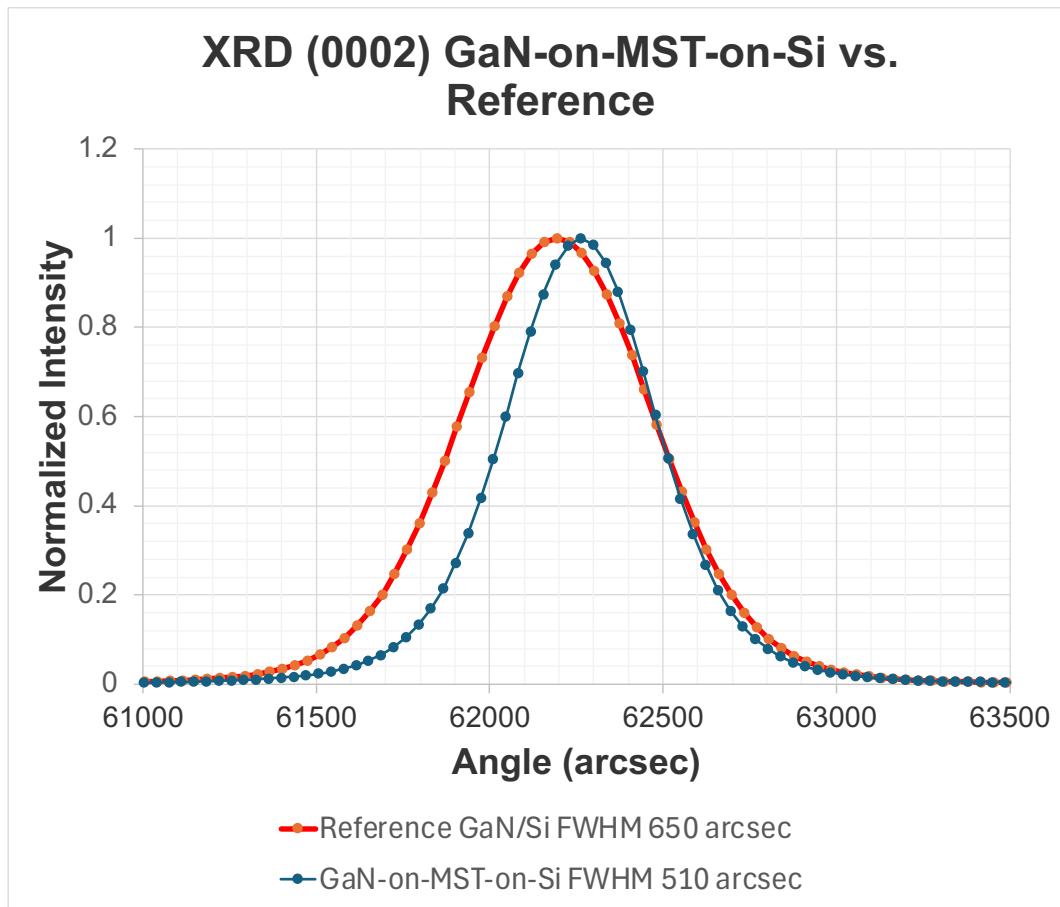


Figure 4: MST improves Texas State reference GaN stack by > 20% as measured by XRD FWHM. Reference wafer [0002] FWHM is 650+/- 10 arcsec. Best MST wafer improved this to 510 arcsec.

Similar magnitude improvements were also measured for the asymmetric XRD [0014] signal, and also for the AlN nucleation layer itself.

Reducing the Parasitic Channel

The quality of the AlN layer is known to be important for controlling the parasitic channel by reducing Ga migration along dislocations [8]. MST is known to reduce dopant diffusion in silicon for a variety of applications [2,3].

For this reason, Atomera has recently focused on improving RF GaN-on-silicon by reducing the parasitic channel.

Spreading Resistance Probe (SRP) and Secondary Ion Mass Spectroscopy (SIMS)

SRP and SIMS are the two metrologies often used to characterize the parasitic channel from a physical and DC electrical perspective. While SIMS provides the total concentration of elements as a function of depth, SRP measures the local resistance due to the presence of charges. Not all the dopants are electrically active, so SRP gives a better insight into the local conductivity due to the parasitic charge. A result showing lower carrier concentration or interface charge indicates improved RF loss, which is expected to lead to better linearity.

A wide range of MST stacks were grown on high resistivity silicon (111) substrates and sent to Texas State for GaN stack growth. It was found that all the MST structures showed substantial reduction in the interface charge, even those that had not shown significant XRD improvement.

One example, for the best-performing MST as determined by XRD, is shown in Fig. 5 compared to the same AlN/GaN stack grown on a bare high-resistivity silicon reference wafer.

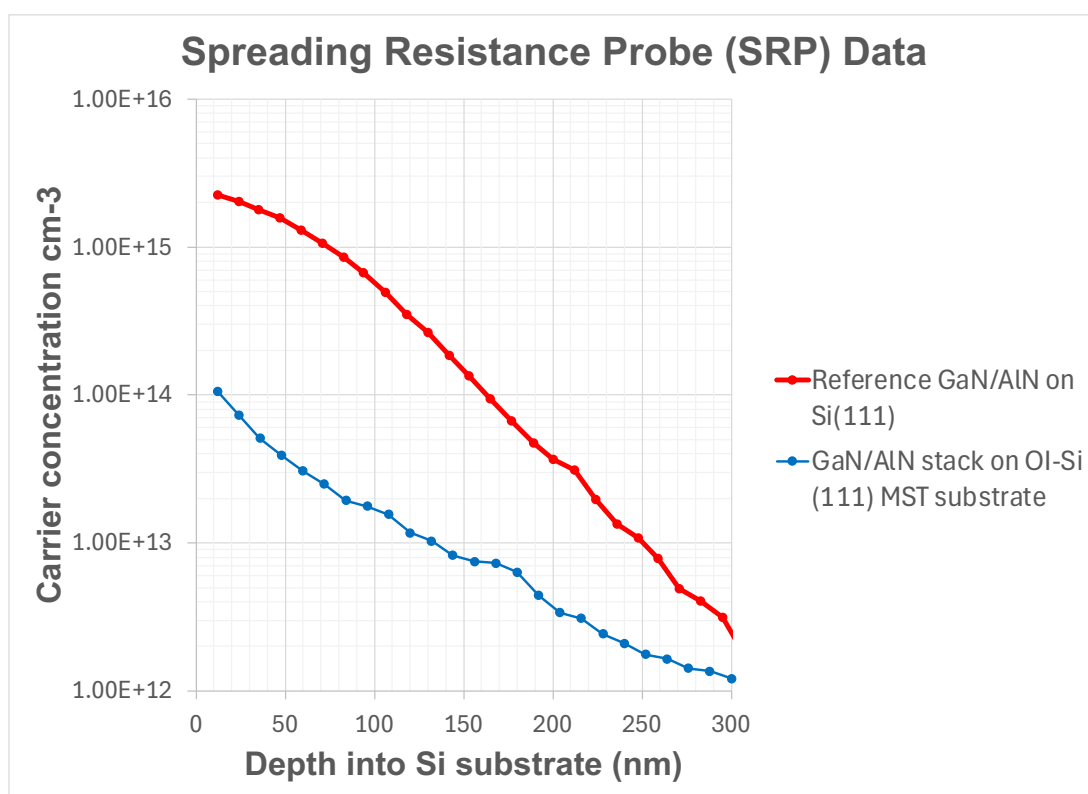


Figure 5. SRP comparison of same AlN/GaN stack grown on reference high resistivity (HR) silicon (111) wafer and grown on MST-on-HR Si (111).

It can be seen that SRP measures significantly lower interface charge. The integrated sheet charge reduction is more than an order of magnitude.

To better understand the mechanism for the reduction, SIMS was performed from the back side of the silicon substrate (after back grinding). Al and Ga penetration into the silicon were both reduced, but the Ga signal showed a similar fall-off and reduced initial value as that seen in the SRP. The Ga SIMS for the same two wafers in Fig. 5 is shown in Fig. 6.

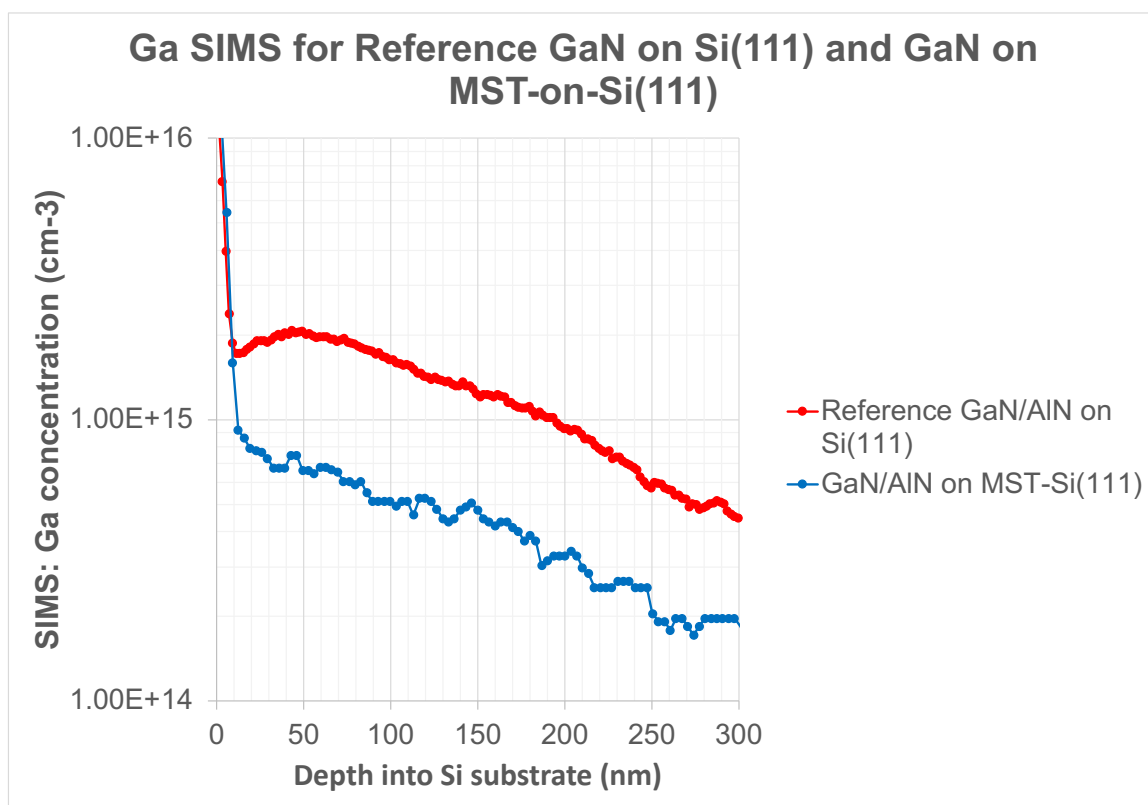


Figure 6: Gallium SIMS for reference and MST wafers shown in Fig. 5.

RF testing collaboration

In July 2025, Atomera announced a collaboration with Incize [9], a Belgium-based company that offers characterization services across the RF industry.

Incize has now characterized the same MST wafers used for the SRP study.

Small-signal RF testing

The first set of RF tests were small-signal RF measurements of coplanar waveguide structures to determine the RF losses [10,11]. The loss was then converted back to an effective wafer resistivity value.

Various wafers were measured. The best-performing wafer split was the same MST structure that showed the best XRD improvement. The RF loss and effective resistivity for two die on the best MST wafer are shown in Fig. 7. Although starting HR Si (111) substrates can have resistivity >10 kΩ-cm, the impact of the parasitic

charge usually reduces the effective resistivity as measured at 900 MHz to around $1\text{ k}\Omega\text{-cm}$, or even lower which is problematic for device implementation due to high RF losses. The exciting feature of the small signal characterization is that the GaN stack grown on MST on HR silicon maintains an effective resistivity above $10\text{ k}\Omega\text{-cm}$ over a wide frequency range. This value is sufficiently high for RF losses to be negligible in most RF applications.

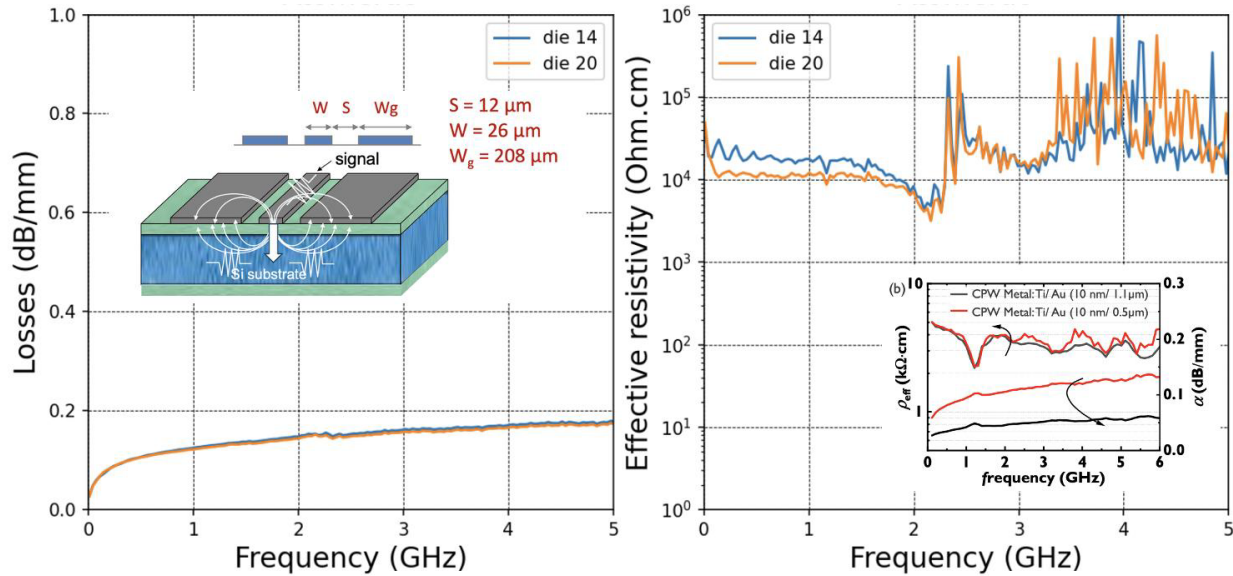


Figure 7. RF losses and effective resistivity as a function of frequency for the best performing MST wafer. The inset on the left figure shows the dimensions of the coplanar waveguide structure used in testing. The right inset shows representative research values for optimized GaN/Si [10].

Large-Signal RF testing

“Lossless” RF transmission for GaN/Si is a big deal, but not the whole story. Depending on the RF application, the linearity of the transmission is also crucial. For mainstream RF front-end circuits in cell phones, for example, the linearity of RF SOI was the key factor in the adoption of RF SOI for RF switches and low-noise amplifiers (LNAs). Linearity is also a key concern for power amplifiers.

The linearity is determined by how much power of the RF signal is found spectrally in the second (symmetric) harmonic (H2) or third (asymmetric) harmonic (M3) as a result of distortion of the fundamental frequency.

For this reason, typical RF benchmarking exercises plot the H2 power in dBm (for an input power of +15 dBm) versus the effective resistivity (measured at 900 MHz). The historic reason behind the frequency test condition is that 900MHz is the fundamental frequency for many wireless standards like GSM. For reference, an input power of 0 dBm is 1mW so +15 dBm is about 30 mW, a reasonable power handling level for many applications. For some applications, though, the linearity at much higher powers in the Watt range (i.e. >30 dBm) is more important.

Large signal testing was conducted at Incize. The H2 and H3 powers were measured as a function of input power ranging from approximately -15 dBm to +40 dBm. The best performing MST wafer had H2 = -96 dBm

and H3 = -115 dBm at an input power of +15 dBm. This is the same wafer with >10 k Ω -cm effective resistivity at 900MHz (16 k Ω -cm). For comparison, the reference GaN/Si wafer had H2 = -67dBm and H3 = -87dBm. In other words, both the H2 and H3 powers for the MST wafer were about 1000x lower than the reference wafer! A plot of the H2 and H3 power versus the input power (in dBm) for the best performing MST and the control GaN/Si wafer is shown in Fig. 8.

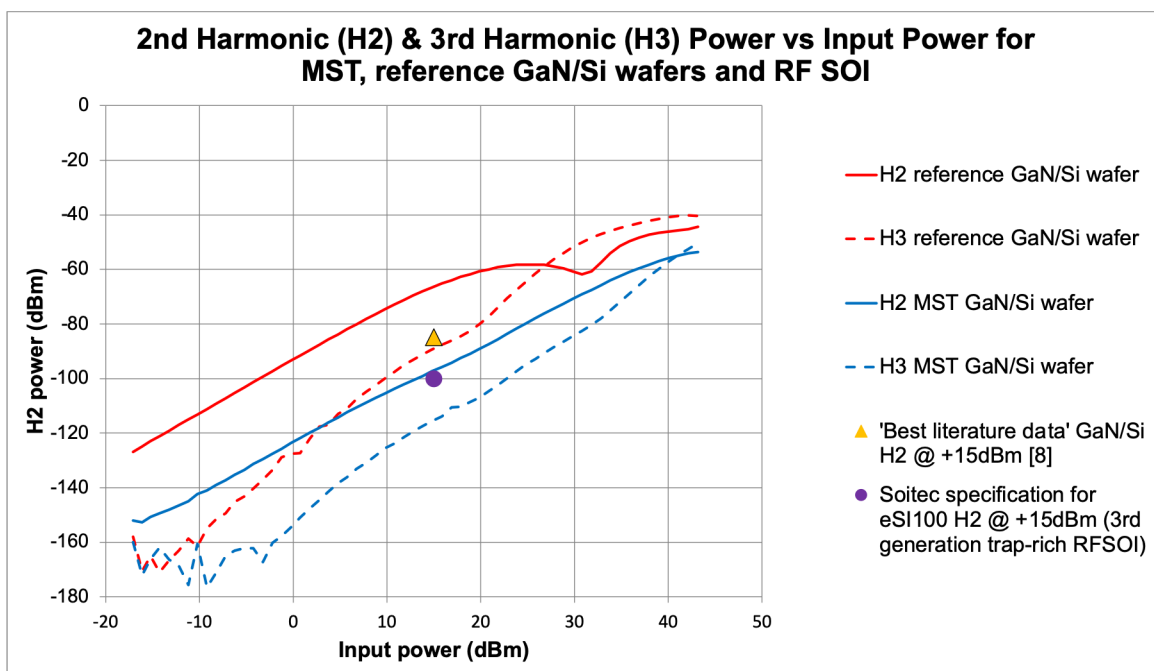


Figure 8: Plot of H2 and H3 power versus input power (in dBm) for MST GaN/Si, reference (control non-MST GaN/Si) wafer and other key comparative data.

These data represent an outstanding improvement in linearity for the standard test conditions used to compare RF technologies. Perhaps even more important, the near ideal linearity of the MST-enabled GaN/Si devices extends into the high-power regime. The best-performing MST die have H2 and H3 power ~95dB lower than the input power for input powers beyond +40dBm.

Another way of visualizing the data is to plot the H2 power at an input power of +15dBm against the effective resistivity measured at 900MHz. The general trend is that lower H2 and improved effective resistivity go hand in hand. This kind of plot is a convenient way to benchmark different technologies. One such comparative plot, based on data previously prepared by Incize, and including the latest MST data is shown in Fig. 9.

The Texas State reference wafer does not include all the latest learning on interface engineering. But even compared to “record-low” literature data [8], the MST wafer has >2x higher resistivity and >15x lower H2 power, taking MST GaN/Si to the heart of mainstream RF benchmarks for trap-rich RF SOI.

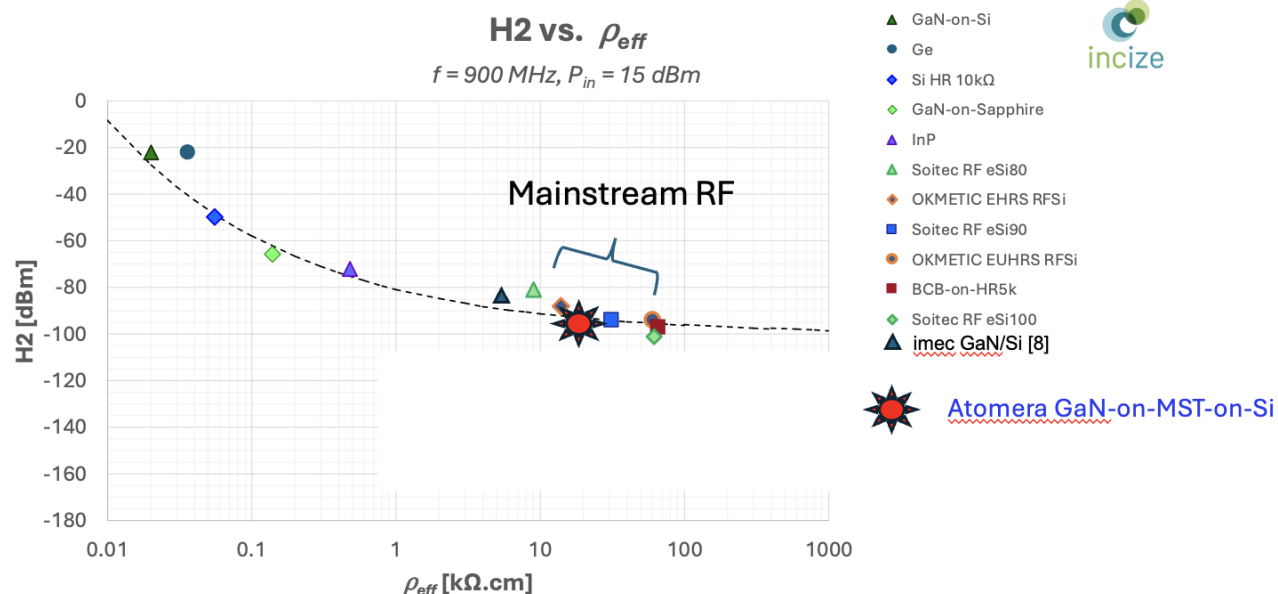


Figure 9. Benchmarking plot of various RF technologies. The latest MST RF data puts GaN-on-MST-on-silicon in the mix of mainstream RF technologies in use today.

Conclusions

While there still remains further characterization and productization work to do, it is clear that MST has the potential to bring RF Ga/Si into the forefront of mainstream RF applications across a broad range of technologies. We are working on further improvements to MST and the AlN/GaN interface and believe further co-optimization will unlock even greater value.

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