

White Paper:

MST-SP 5V PMIC Power Device

Pushing the Industry's Leading Performance Higher

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Introduction

In 2022, we launched our MST-SP® (smart profile) product, an asymmetric 5V power device for PMIC and other applications (details are available in the Atomera white paper, “MST® for PMIC and RF-SOI Switches”). After the initial announcement and a follow-up publication in the IEEE International Symposium on Power Semiconductor Devices (ISPSD) [1], we have continued our efforts and further improved the device performance (Figure 1) to extend MST-SP’s lead over all other 5V power switches. In this white paper, we review the design concept of our MST-SP device and elaborate how MST doping profile control helps the device scale.

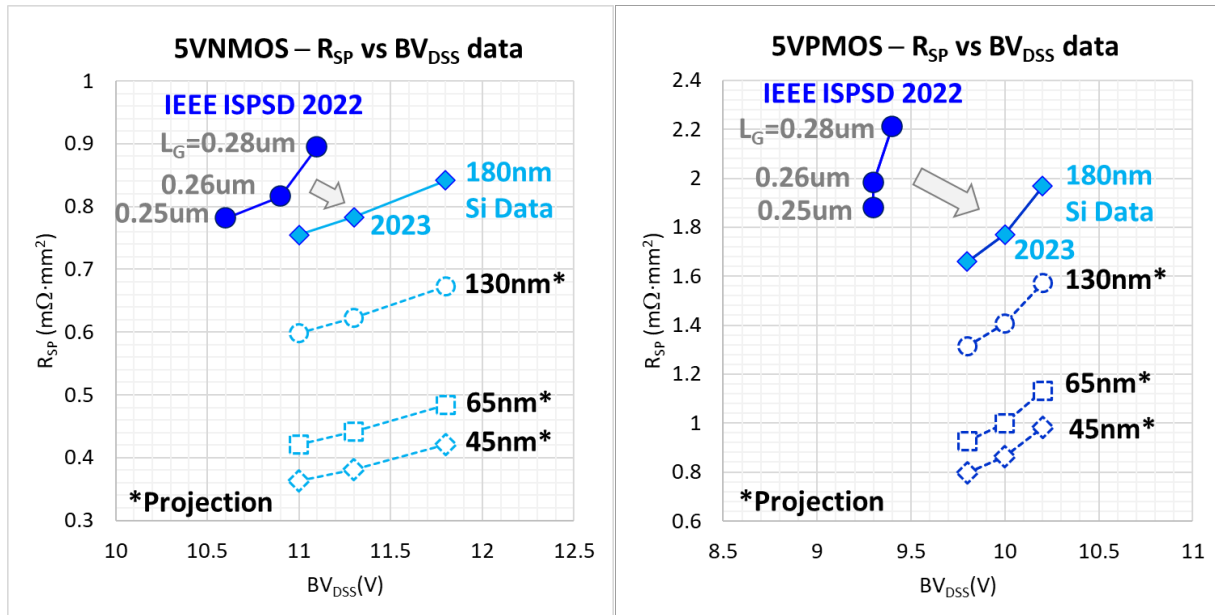


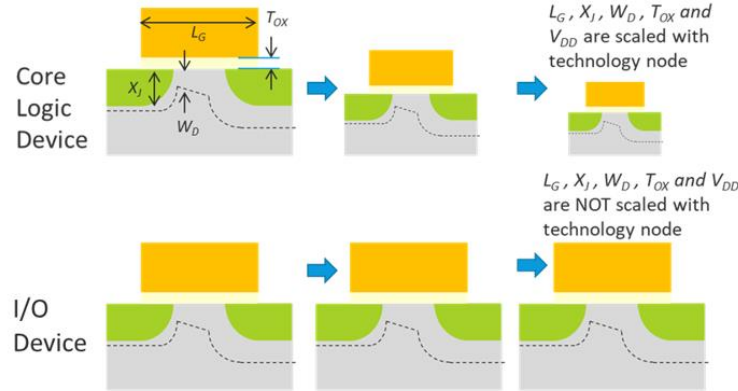
Figure 1: R_{SP} vs. BV_{DSS} of (a) NMOS and (b) PMOS MST-SP devices. MST-enabled “best-in-class” 5V power switch performance published^[SB1] in IEEE ISPSD 2022 [1] has been further improved. Projections in 130nm, 65nm, and 45nm nodes were made by scaling contact size and pitch extrapolated from the 180nm Si design rule assuming that $R_{DS(on)}$, BV_{DSS} , V_{DSMAX} , SOA are maintained.

MST-SP device design concept

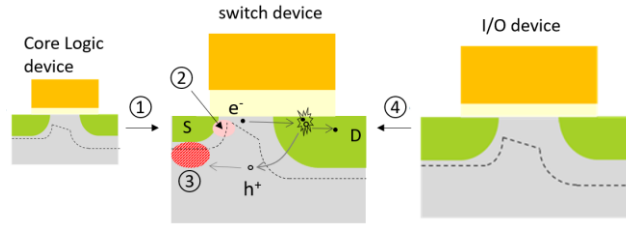
PMIC chips consist of core logic devices, analog devices, and power switches. The MST-SP power switches are based on the baseline I/O device, but with a change from the symmetric source/drain profile to an asymmetric design to meet the various specification requirements. Power switches are generally required to handle higher voltage than the baseline I/O device. For higher voltage devices, drain engineering plays a key role, since the high voltages applied to the drain introduce challenges in simultaneously meeting the requirements of breakdown voltage, HCI (hot carrier injection) reliability, and SOA (safe operating area). On the other hand, mobile products use low-voltage power switches for Li-ion batteries with a lower voltage range (2.5-4.2V) than the baseline I/O device (5.0V). The MST-SP device targets such low-voltage power switches. We took a different approach from conventional power switch design, focusing on source engineering while keeping the drain side doping scheme unchanged from the baseline I/O device.

Conventional L_G scaling of core devices has been driven by lithography, following Dennard's law [2] to reduce T_{OX} , X_J , and W_D in each technology node. On the other hand, the geometry of 5V I/O devices has remained largely unchanged across the generations (Figure 2(a)). Our source engineering concept of the asymmetric source/drain device focuses on this gap. Since MOSFET's turn on via source-side carrier injection, reduction of X_J and W_D on the source side helps L_G scaling for controlling short channel effects. The core LDD process in the same process platform has been established to achieve shallower X_J , and narrower W_D can be obtained by implementing a source-only halo implant.

In addition to short-channel control, challenges specific to power switches regarding maintenance of breakdown voltages, HCI reliability, and SOA must be overcome while scaling L_G . For SOA improvement, the key is to mitigate impact ionization and efficiently collect generated holes. A shallow p-well under the source is effective due to a reduction of body resistance in the hole current path (Figure 2 (b)).



(a) L_G scaling of core device via shrinking L_G and characteristic length, $l = \sqrt[3]{T_{OX} \cdot W_D \cdot X_j}$



(b) MST-SP source engineering concept for low-voltage power switch scaling

Figure 2: (a) Conventional Dennard's Law for L_G scaling driven by core logic devices; (b) Source engineering concept for L_G scaling of low-voltage power devices: ① implementation of shallow LDD process of core devices; ② halo optimization for W_D scaling and V_T control; ③ source-side shallow p-body for SOA retention; ④ maintaining baseline drain doping process for retention of SOA and reliability.

MST 2D doping profile control for Source Engineering

MST doping profile control mitigates the key challenges of BV, HCI, and SOA for L_G -scaled power devices. The MST film blocks diffusion of dopant atoms via interactions with point defects. This unique feature is not limited to the depth direction but is effective in the lateral direction as well. Figure 4 compares SCM (scanning capacitance micrograph) images of a Si control device and an MST device, to visualize the difference in 2D doping profiles of the two devices. The SCM images clearly show that the MST device yields longer L_{EFF} than the Si control for both NMOS and PMOS, due to retarded lateral dopant diffusion with the presence of the MST film near surface.

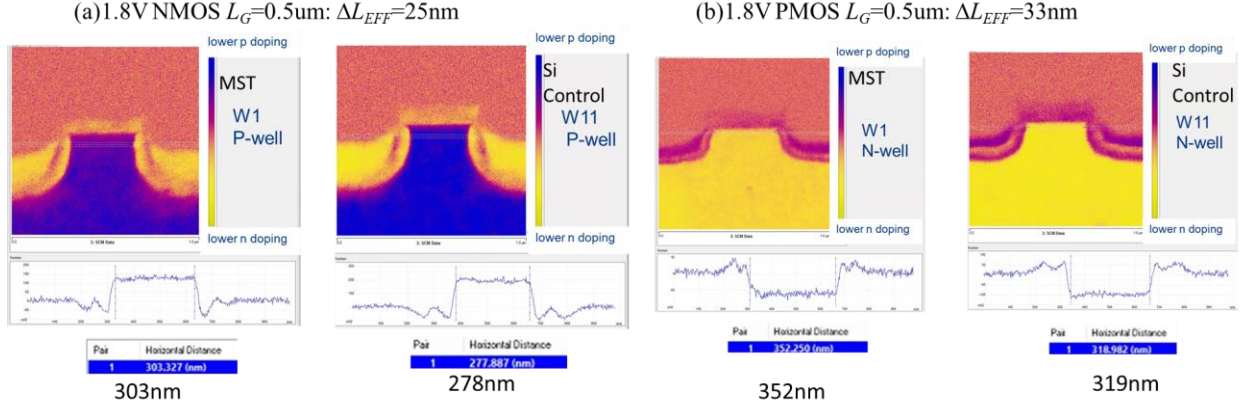


Figure 3: SCM (scanning capacitance microscope) images of (a) NMOS, $L_G=0.5\mu m$; (b) PMOS, $L_G=0.5\mu m$ for Si control and MST devices. Top 2D images show doping profiles and the bottom line-profiles show measured doping level at the channel surface, from which L_{EFF} (effective gate length) were extracted as the distance between two metallurgical junctions. For both NMOS and PMOS, MST devices exhibit longer L_{EFF} than the Si control.

The observed L_{EFF} difference induced by the MST film is favorable for the L_G scaling of power switch devices because it is not lithography and patterning technologies but BV, HCI, and SOA that limit the shortest L_G applicable for the power switch devices. In particular, SOA is dominated by impact ionization at high drain bias due to the strong lateral electric field in accordance with shrinkage of the physical gate length. Maximum lateral electric field, E_{MAX} is set by the saturation voltage, V_{DSAT} , which in turn is set by velocity saturation of channel electrons in the pinch-off region. The relation is expressed as a function of L_{EFF} via the following formula [3]:

$$E_{MAX} \approx \frac{V_D - V_{DSAT}}{\sqrt{3T_{OX}X_J}} \quad (1)$$

$$V_{DSAT} \approx \frac{(V_G - V_T) \cdot L_{EFF} \cdot E_{SAT}}{(V_G - V_T) + L_{EFF} \cdot E_{SAT}} \quad (2)$$

where E_{SAT} , critical lateral field for electron velocity saturation in the channel is $2 \times 10^4 V/cm$. Accordingly, longer L_{EFF} reduces E_{MAX} at the same L_G , V_G , V_T , and V_D and thus mitigates impact ionization. Combined with effectiveness of boron profile control of the shallow p-well described above, MST can extend SOA-limited L_G scaling.

Figure 4 (a) compares L_G vs. SOA for the Si control and MST devices. Whereas the Si control SP-device scales L_G down to $0.27\mu m$, the MST device can meet the SOA spec at $L_G=0.25\mu m$, while maintaining comparable V_{DSMAX} for HCI reliability (Figure 4 (b)). Notably, HCI is determined by $I_{SUBMAX} = I_D \times [\text{impact ionization rate}]$. Since MST reduces E_{MAX} by longer L_{EFF} and thus impact ionization rate, it allows higher I_D and thus lower on-resistance while maintaining the HCI reliability. As a result, MST enables 18% reduction of specific resistivity, R_{SP} compared to the Si control with the same SP-device doping scheme (Figure 4 (c)).

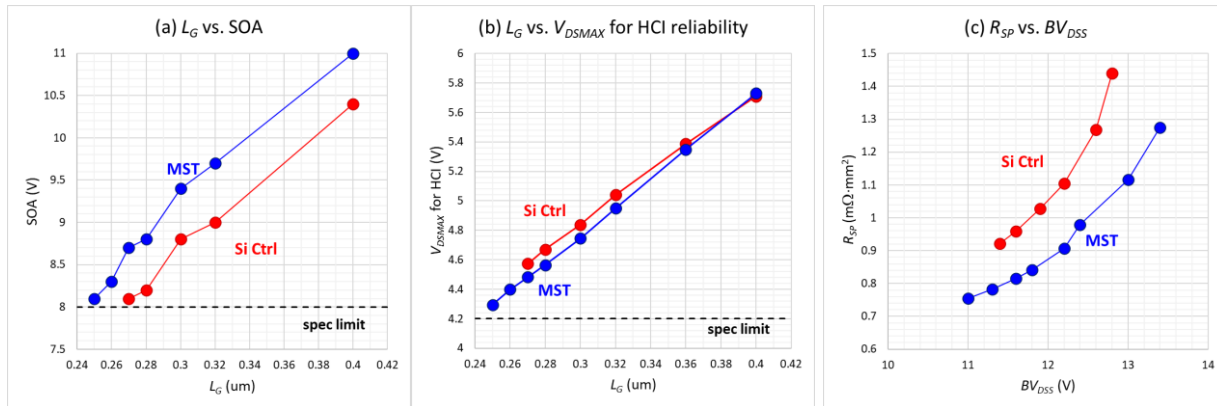


Figure 4: (a) L_G vs. SOA; (b) L_G vs. V_{DSMAX} for HCI reliability; (c) R_{SP} vs. BV_{DSS} for MST and the Si control SP-devices fabricated in a 180nm foundry technology.

Implant Optimization for Continuous Improvement

The original SP-device development work was performed under a constraint that well implant and drain-side LDD conditions are unchanged from the baseline condition of the foundry partner. However, we noticed that BV_{DSS} of the SP-device was limited by drain junction breakdown associated with the baseline well implant process. For further improvement, we revised the well implant condition and source-side LDD and shallow p-well implant conditions. As a result, we were able to achieve a 3%/0.4V and 12%/0.5V of R_{SP}/BV_{DSS} improvement for NMOS and PMOS MST-SP devices, respectively, compared to ISPSD 2022 data, as shown in Figure 1. It should be noted that the implant process change from the baseline does not increase mask counts and that the performance of regular symmetric I/O device is unaffected because well implant change was made to modify doping profile under deep source/drain region for BV_{DSS} improvement.

Summary and Future Work

The MST-SP device was designed as a power switch for Li-ion battery applications, based on a source engineering concept for L_G scaling. MST's unique dopant profile control feature enhances the L_G scaling while maintaining BV, HCI, and SOA requirements for scaled devices. Our results in 2022 demonstrated that MST-SP was the industry's best-in-class power switch device. Our further optimizations have extended this lead, especially in the PMOS device – demonstrating up to 30% lower N-device R_{SP} , up to 40% lower P-device R_{SP} , with L_G 20%-40% shorter than competitive offerings. These improvements mean that MST-SP provides even higher cost savings and power reductions versus conventional technologies.

MST dopant profile control will be effective for drain engineering of higher voltage power switch devices as well. Work is in progress and will be reported soon.

References

- [1] Y. -A. Chen et al., "Source engineering on Oxygen-Inserted Si channel for gate length scaling of low-voltage switch devices", 2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 197-200, 2022.
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