MST®-SPX 7-48V Power Device Performance Projection

Breaking through the classical Si limit

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In 2022, we launched our MST-SP® (smart profile) product, an asymmetric 5V power device for PMIC and other applications (details are available in the Atomera white paper, "MST® for PMIC and RF-SOI Switches") followed by a publication in the IEEE International Symposium on Power Semiconductor Devices (ISPSD) [1]. In 2023 November, we reported further device performance improvement (details are available in the Atomera white paper, "MST-SP PMIC Power Device") to extend MST-SP's lead over other 5V power switches. The MST-SP device targets low voltage (2.5-4.2V) Li-ion battery applications for mobile products. We started from the baseline 5V I/O device and focused on the scaling of physical gate length via source-side dopant engineering without changing the baseline process on the drain side.

For higher voltage switches, the structure on the drain side, called the "drift region", must be modified to handle higher supply voltages. Hence, "drift engineering' is the key for performance improvement of these devices. Here, we report our progress on MST-SPX® (smart profile extension) device development via MST drift engineering in conjunction with established source engineering as demonstrated in the MST-SP device. MSTcad® simulations project that the key metric R_{SP}-BV_{DSS} characteristic of the MST-SPX device not only exceeds the quoted values from top chip makers [2]-[5] but also the classical (1D) limit of Si power devices [6] (**Figure 1**).

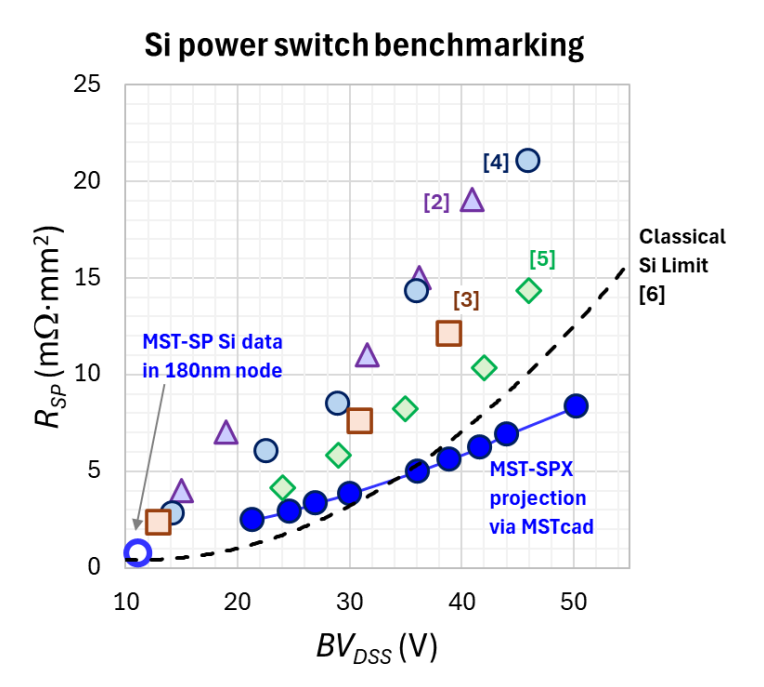

Figure 1: Bench marking of Si power devices.

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Background – the challenge of sustaining breakdown voltage with high drain voltage

In 1979, Prof. Chenming Hu at UC-Berkeley derived the optimum doping profile of a lightly doped layer to achieve the minimum series resistance while sustaining a given junction breakdown voltage for a one-dimensional Schottky diode and found that the optimum doping profile can be closely approximated by a uniformly doped n-n + structure [6]. Switch devices having additional resistance components in the source and the channel regions could not have surpassed the derived relation of resistance *vs.* breakdown voltage for a long time. Hence, the derived formula has been used as the "ideal Si device" for benchmarking of R_{SP} vs. BV performance.

In the same year (1979), a group from Phillips proposed a RESURF (reduced surface field) technology for lateral high-voltage diodes [7]. The (two-dimensional) RESURF reduces the surface electric field at the high-voltage drain contact by designing the vertical doping profile to deplete the drift layer, sustaining a high voltage at the bottom of the junction via a wide depletion layer. The RESURF technique provides an efficient way to integrate high-voltage transistors with low-voltage digital or analog circuits and thus has been widely adopted for power devices.

Transistor structures having a gate electrode need to overcome an additional challenge. The high electric field induced at the gate edge due to coupling of the electrostatic potential between the drift layer and the gate electrode degrades breakdown characteristics. To alleviate the gate-edge high field, high-voltage transistors implement thicker oxide than the gate oxide at the drain edge. There are a couple of options for thick oxide. In one configuration, shallow-trench isolation (STI) is inserted between the channel and the drain. In another configuration, the STI isolation is replaced by local oxidation of silicon (LOCOS). In another configuration, LOCOS is replaced with "step gate oxide" which is formed by depositing and patterning CVD oxide on the regular gate oxide. In more recent device configurations, an additional electrode is added as "Field Plate" in the drift region to further control electrostatic potential of the drift layer at the gate edge [8].

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MST-SPX drift engineering

The doping profile control capability of MST can be used to engineer the drift region for performance enhancement of power devices. MST can increase phosphorus concentrations in the surface region of the drift layer due to dopant pile-up into the MST layer and dopant retention via diffusion blocking. **Figure 2** shows the phosphorus SIMS profile change by the MST layer. It can be seen that insertion of the MST layer leads to creation of a peak near the surface to a uniformly doped drift profile. The surface peak improves drift resistance due to sheet resistance reduction in the main electron conduction path. When the RESURF doping profile is appropriately designed, the surface peak in the drift layer does not degrade breakdown characteristics.

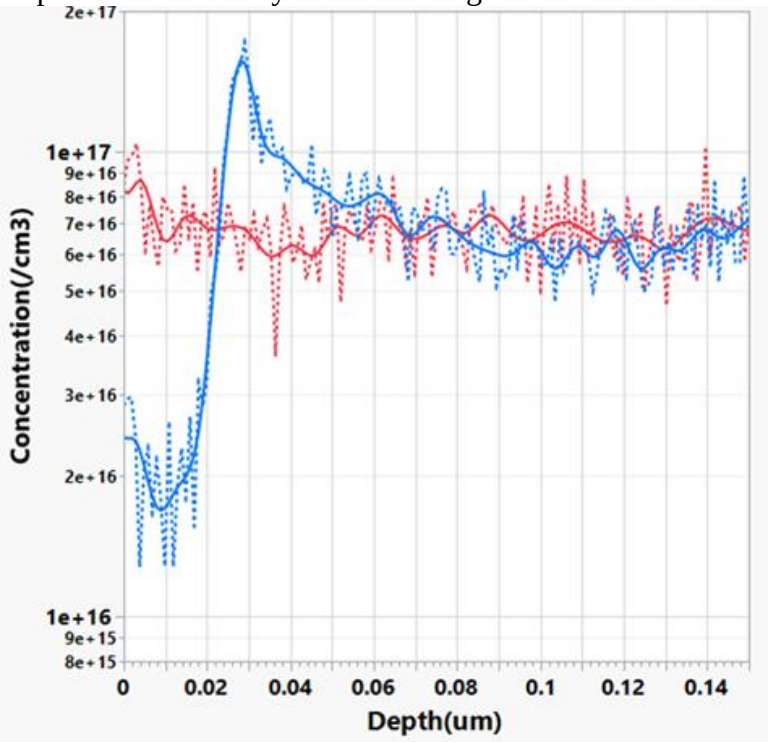

Figure 2: Comparison of drift layer phosphorus SIMS profile for Si control and MST.

To see its effectiveness, MSTcad® simulation was performed using the deck calibrated to a 180nm process and validated via MST-SP Si data (**Figure 1**). A drain-extended NMOS device with 5V gate oxide, step gate oxide, and field plate was studied. **Figure 3** compares R_{SP}-BV_{DSS} characteristics for MST-SPX and Si control. L_{DEVICE} (total poly-Si length including channel and drift overlap regions) was varied with the same implant conditions to cover a wide BV_{DSS} range. The same implant conditions were used for MST and Si control for drift and RESURF layers. The same implant energy was used but implant dose was varied for P-body layer to achieve the same V_T. MST improves R_{SP} by 8-20% for 10~50V of BV_{DSS} range. The projected R_{SP} exceeds the "classical Si limit" for BV_{DSS}>36V. It should be noted that the classical Si limit approximated by uniform doping profiles was calculated using a 1D model for simple two-terminal device whereas MSTcad simulations were performed using a 2D model implementing RESURF and Field Plate technologies with high surface drift doping in the electron conduction path.

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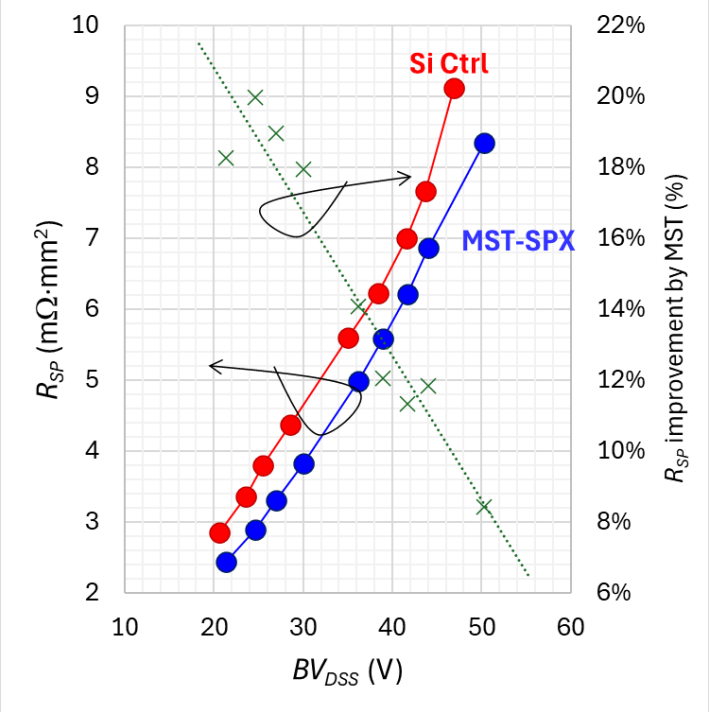

Figure 3: Comparison of simulated R_{SP} vs. BV_{DSS} for Si control and MST.

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Effectiveness of MST-SP source engineering

MST source-side engineering learned during MST-SP development can further enhance the performance of high-voltage power devices. While BV_{DSS} is the breakdown voltage for the off-state, at V_G=0V, power switch devices also need to sustain breakdown in the on-state due to the onset of parasitic BJT conduction. The *On-BV* is lower than BV_{DSS} and thus limits the operating voltage of the switch device. Reducing the body resistance improves the *On-BV*, since holes generated by impact ionization, which trigger tuning on the parasitic BJT formed between source and drain, can be efficiently swept away to the body contact. MST enables a body-resistance reduction via the dopant diffusion blocking effect. The MST layer prevents up-diffusion of boron and thus allows higher boron concentration under the source while retaining the target V_T. **Figure 4** compares R_{SP} vs. *On-BV* characteristics for MST-SPX and Si control. MST-SPX can improve the *On-BV* by 2-4V to increase operation margin, or, more aggressively, improves R_{SP} more than 25% at the same *On-BV*.

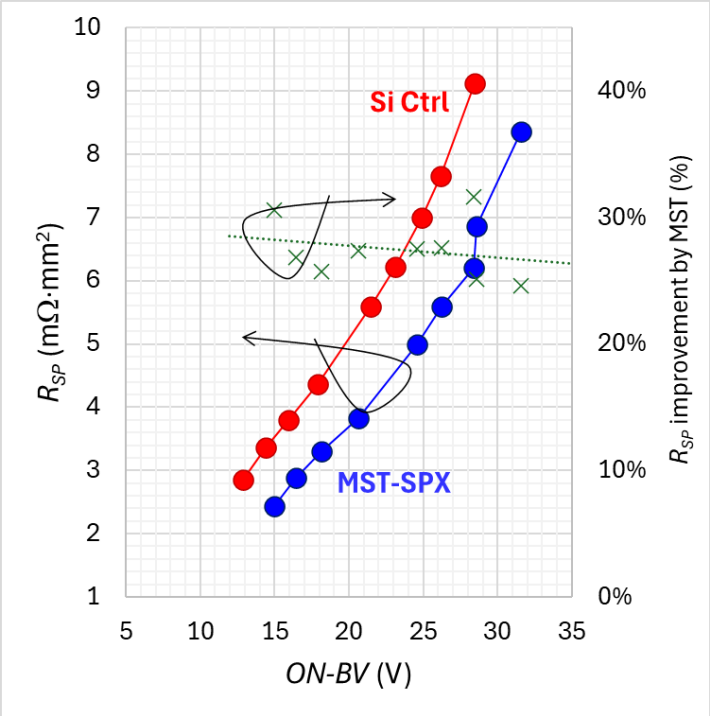

Figure 4: Comparison of simulated R_{SP} vs. *ON-BV* for Si control and MST.

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Summary and Future Work

We have reported the progress of our work on the MST-SPX device. MST drift engineering enables 8~20% improvement in the key R_{SP}-BV_{DSS} characteristics by increasing surface doping concentration in the electron conduction path. MST source engineering helps improve *On-BV* by 2~4V or R_{SP} by >25% at the same *On-BV*. MST drift and source engineering combined with step oxide, field plate, and RESURF doping optimization, is projected to enable R_{SP} to exceed the classical 1D Si limit for BV_{DSS}>36V.

Work is in progress to validate the effectiveness of this design in silicon as well as to extend the applicable voltage range up to 48V.

References

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