



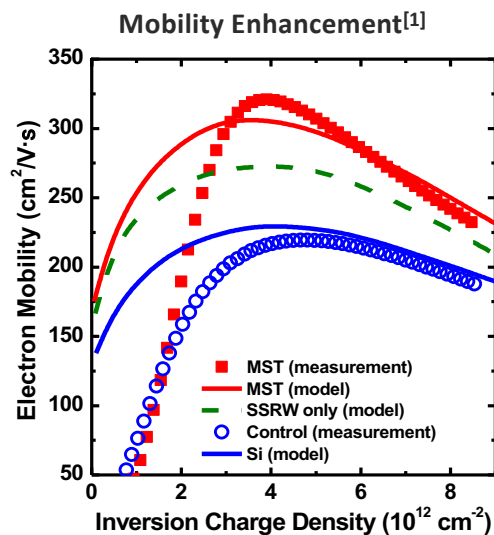
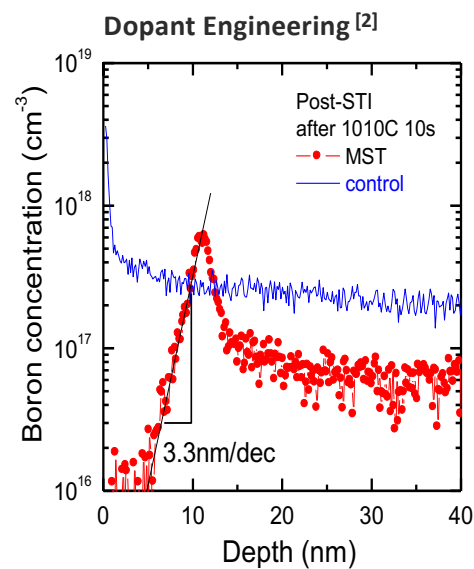
atomera

MST[®] for RF-SOI

Robert Mears

Atomera Inc

MST[®] : Mechanism and Benefits



Toolbox for NMOS and PMOS

- I_{dlin} , I_{dsat} and G_m enhancement
- Gate Leakage reduction
- Precision Doping Profiles
- Variability reduced & Matching improved
- TDDDB & NBTI Reliability improved

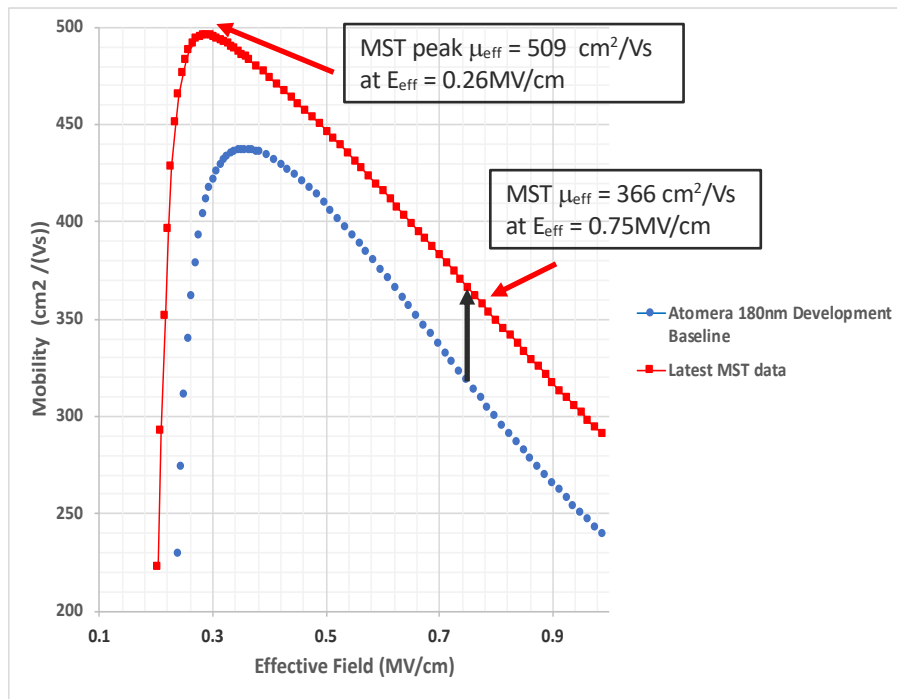
[1]: N. Xu et al., "Electron mobility enhancement in (100) oxygen-inserted silicon channel," APL 107, 123502 (2015)

[2]: R.J Mears et al; "Simultaneous carrier transport enhancement and variability reduction in Si MOSFET by insertion of partial monolayers of Oxygen", IEEE VLSI Tech Symp. 2012

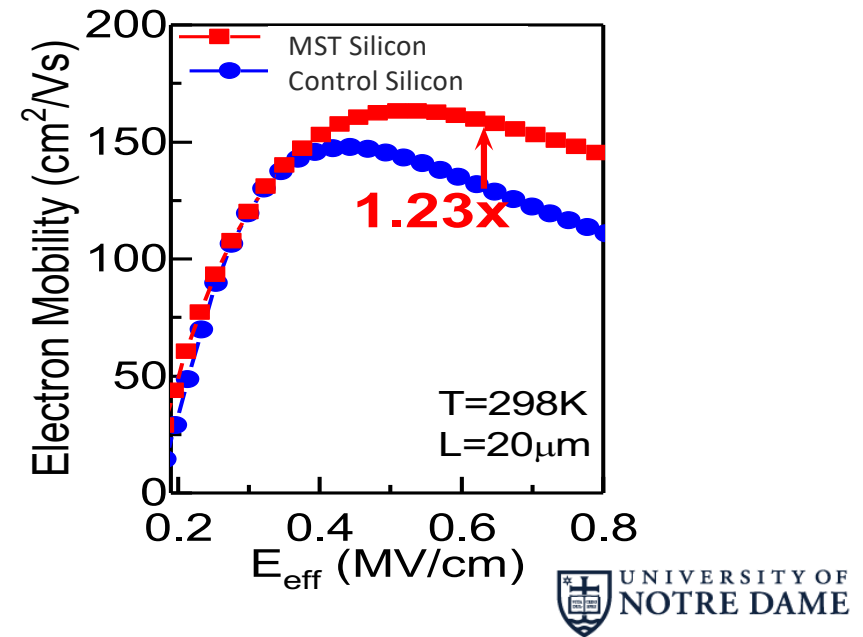
MST Mobility across nodes / technology



Silicon results from 180nm Flow

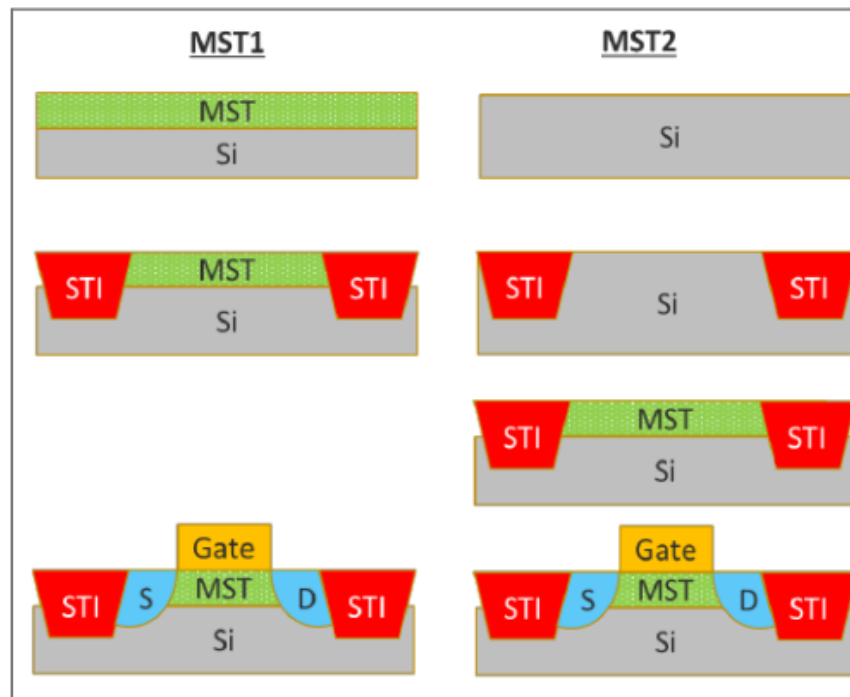


MST Mobility for HKMG Flow



Ref: 2018 IEEE 978-1-5386-3028-0/18 ; JA Smith, S. Datta et al

Integration of MST in Process Flow



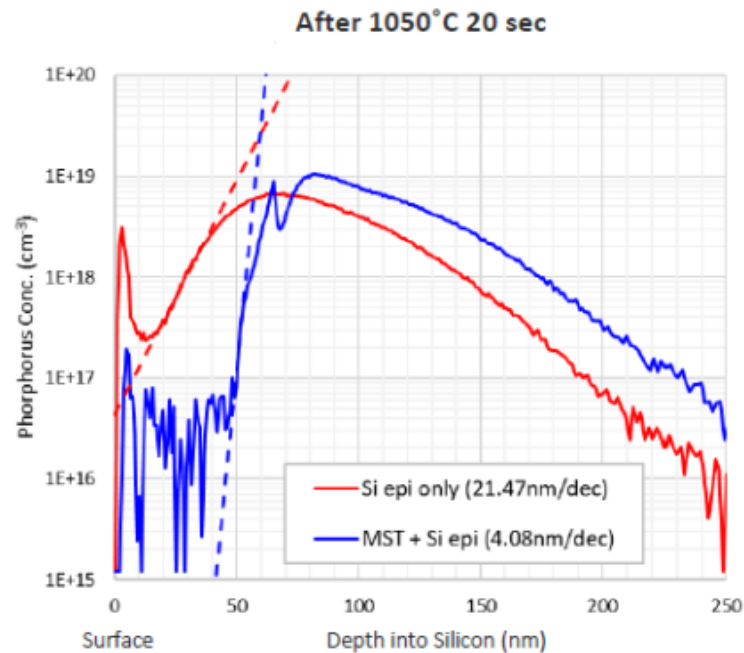
MST1

- Blanket film
- Cheapest integration
- Best suited for Low DT processes
- FinFET; RF SOI; etc.

MST2

- Selective growth
- Provides flexibility
- Avoids higher DT processes
- DRAM; HKMG; Power; etc.

Dopant Diffusion Blocking by MST



MST blocks up diffusion of Phosphorus

- Up to 5x better than control (Si epi)

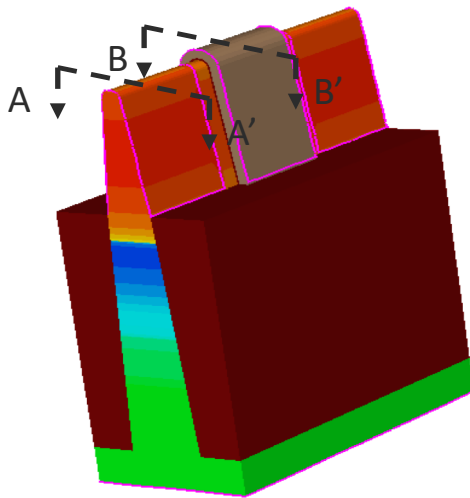
Proven for multiple dopants

- Phosphorus
- Boron
- Arsenic

Compelling results for Advanced 3D Logic

MST for FinFET

14nm FinFET Technology Analysis*



Technology Integration

- Punch Through Stopper (PTS)
- Dopant Profile engineering

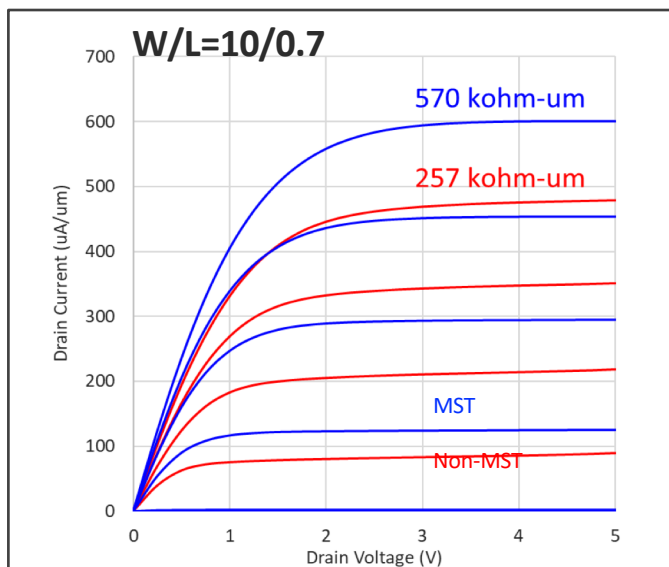
Performance Improvements

- I_{DLIN} 21 %
- I_{DSAT} 10%
- Improvement in $\sigma_{V_{Th}}$ and A_{VT}

MST for Analog



Results from Silicon testing of 180nm BCD technology



5V Analog transistor with MST®

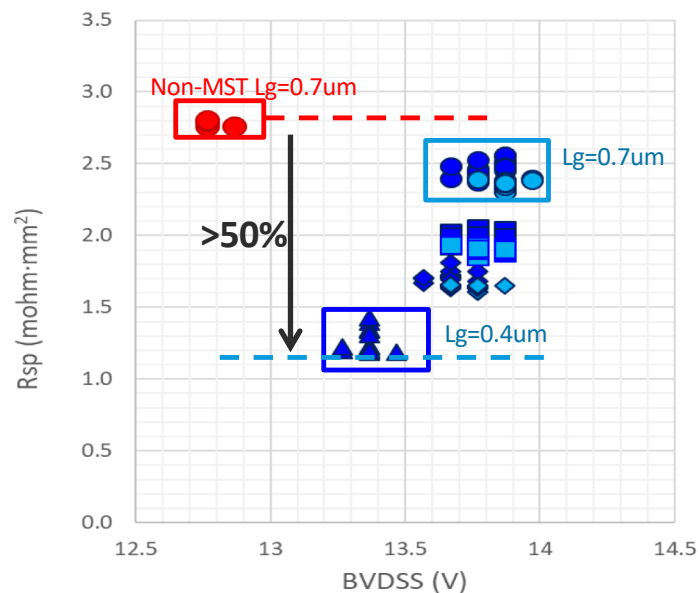
- Gm 30%
- Rout 122%
- Gm*Rout 189%
- Matching > 50%

MST® improved Analog performance of 5V transistor

MST for Power (BCD)



Silicon results for 5V Power Switch



MST[®] enhances 5V Power Switch

- R_{sp} reduction by > 50%
- BV_{dss} improved by $\sim 1V$
- I_{submax} (HCI) – equal or better
- Enables Gate Length scaling

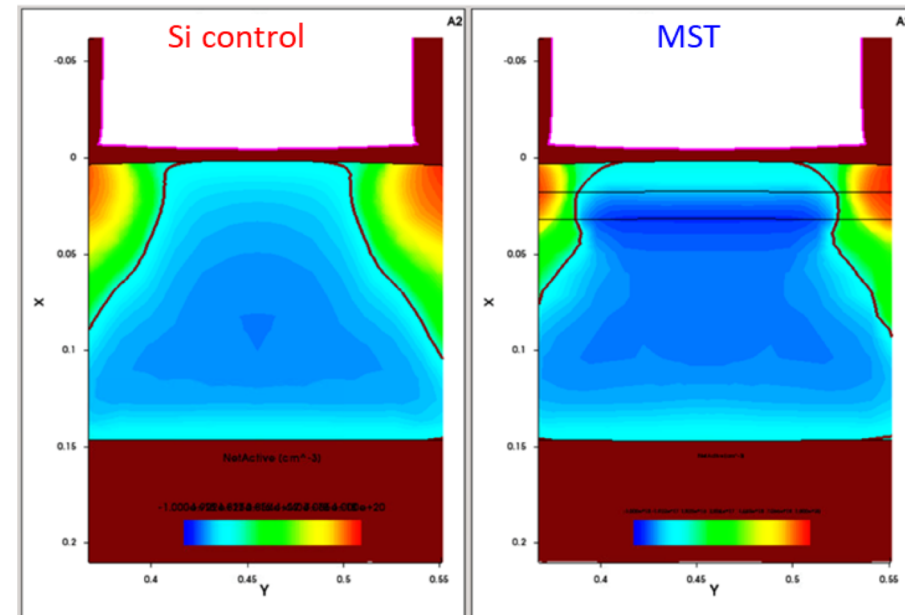
Reduce PMIC die size by up to 25% with MST[®]

MST RF SOI: TCAD Simulation



MST allows greater Boron retention in thin silicon-on BOX by blocking oxidation enhanced diffusion (OED) during gate oxidation

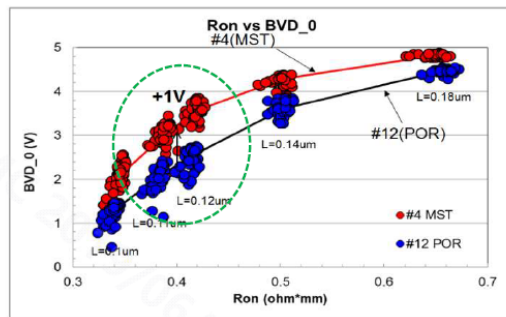
MST dopant engineering allows further degree of freedom for RF-SOI device optimization in addition to mobility-driven Ron benefit



MST Silicon Data: RF Switch performance



Switch FET Data



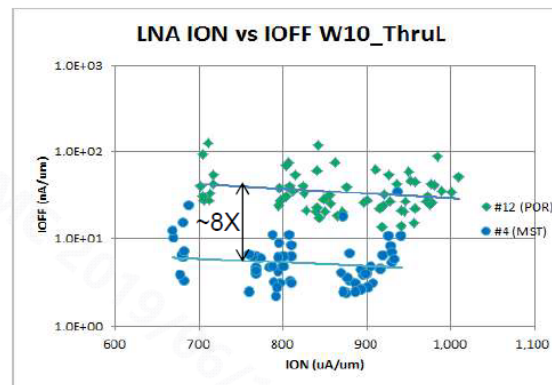
BVD_0V Versus Ron

Improved BV and Ron

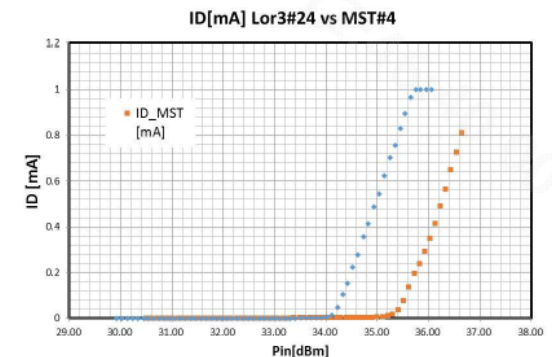
- BV: Up to 1V for same Ron
- Ron: Up to 20% reduction at same BV

- Silicon results (preliminary) from a major foundry
- MST1 integration without process optimization
- Further improvement can be achieved in :
 - C_{off} → with SOI thickness optimization
 - R_{on} → with Implant/dopant profile optimization

LNA NMOS Device

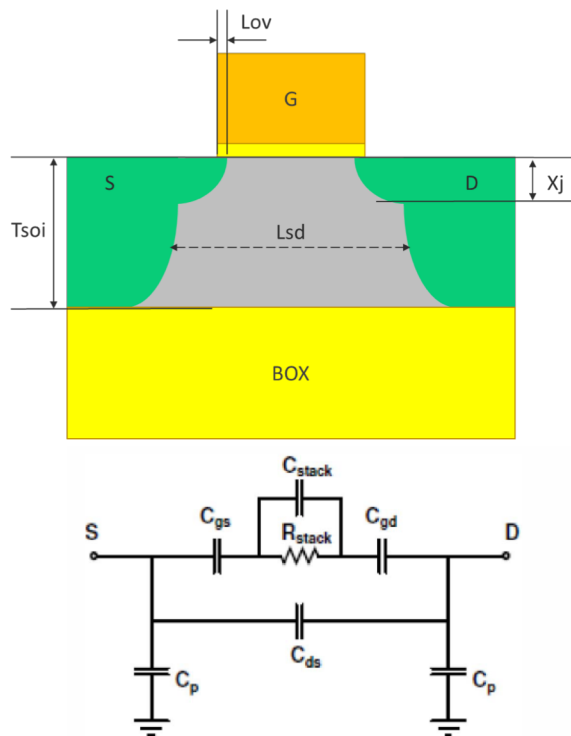
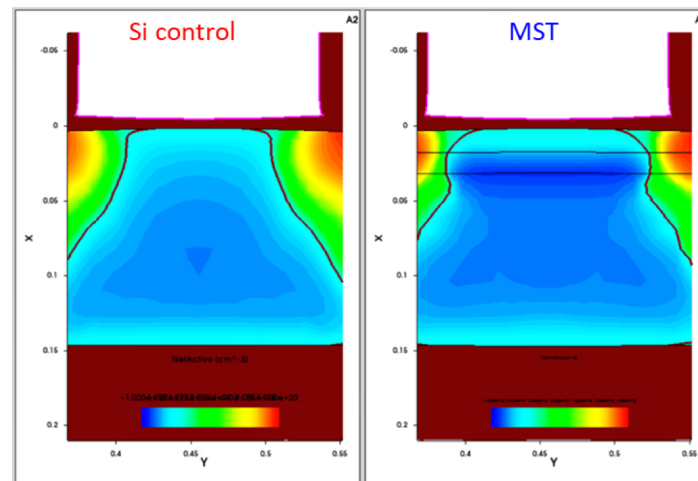


Switch RF Power Handling



• RF Power Handling improved >1dB

Enhancing RF Switch Performance with MST



$$N_A \uparrow \Rightarrow BV_{dss} \uparrow$$

$$N_A \uparrow \Rightarrow L_{sd} \uparrow \Rightarrow C_{ds} \downarrow$$

$$X_j \downarrow \Rightarrow C_{ds} \downarrow$$

$$X_j \downarrow \Rightarrow L_{ov} \downarrow \Rightarrow C_{gs} \text{ \& } C_{gd} \downarrow$$

Summary



- MST[®] is a Toolbox for improving NMOS and PMOS transistors
- For RF-SOI, MST delivers significant Ron-BV improvement and route to further Ron*Coff-BV improvement



atomera

MST[®] for RF-SOI

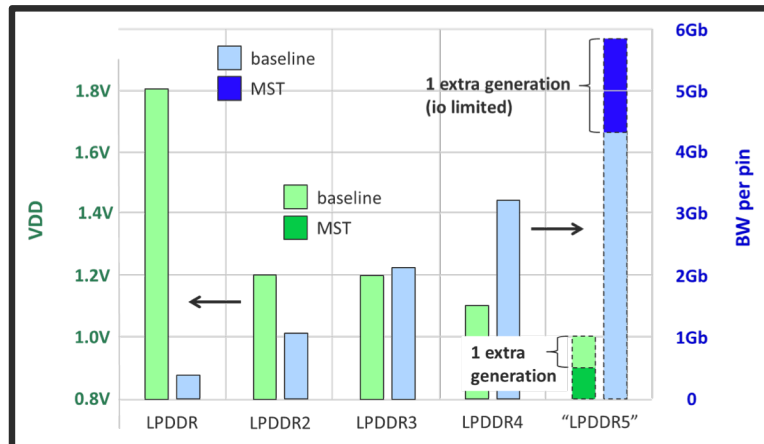
Robert Mears

Atomera Inc

MST[®] for DRAM



Lower V_{dd} & Increased Bandwidth*



- **leff/loff Improvement**
Up to 25% for NMOS & 15% for PMOS
- **TDDDB Improvement**
200mV ~ 300mV overdrive possible
=> 40 ~ 60% boost to NMOS and PMOS
- **Transistor Matching**
Up to 50% improvement

DRAM periphery performance enhanced by MST[®]

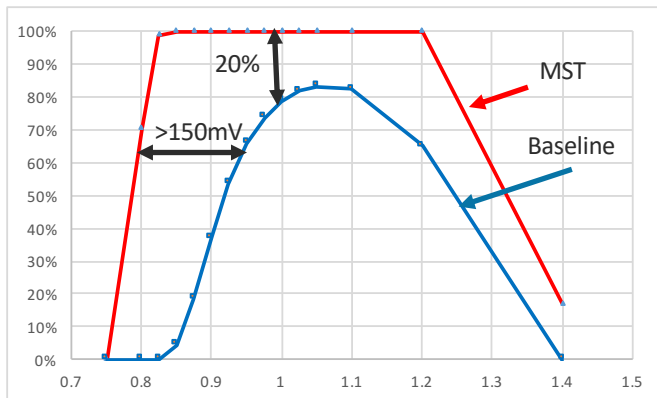
*Note: Analysis performed by a DRAM design consultant

MST® for SRAM & Logic



28nm low-power CMOS Technology Results *

SRAM 1MB Natural Yield without circuit assist



Logic :

- Switching speed up to ~20% at same or lower leakage
- Improved TDDDB allows overdrive capability additional up to 30% boost in switching speed

SRAM :

- V_{min} lower by 100mV ~ 150 mV
- Significant boost in natural and repaired yield

MST® offers up to 1-node improvements for Digital (Logic) Products