

Electron and Hole Surface Roughness Scattering-Limited Mobilities in Oxygen-Inserted (OI) Si Channel

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The electron and hole surface roughness scattering (SRS) -limited mobilities, deconvolved from 4.2 K measurements, were compared between oxygen-inserted (OI) and control Si channel for n- and p-MOSFETs. It was found that electron SRS-limited mobility in the OI-Si channel is 55% higher, whereas hole SRS-limited mobility is comparable to the control. To elucidate the difference, the Si/SiO₂ interface roughness and the nanoscale thickness variation of the gate oxide were analyzed in detail, via high-resolution transmission electron microscopy (TEM) images, and fed into numerical calculation of the SRS-limited mobility. The power spectral densities (PSDs) based on the Yule-Walker autoregressive (AR) model revealed that the OI-Si has a smaller surface roughness at low-frequency components, corresponding to the electron Fermi surface energy level. In contrast, surface roughness improvement was found to be less at a higher frequency region of the PSDs corresponding to the hole Fermi surface energy level. Furthermore, an oxygen tracer experiment identified a dynamic exchange process between the Si/SiO₂ interface and the OI-Si layer, suggesting an opportunity for improving hole SRS-limited mobility in the OI-Si channel via tuning post-oxidation thermal process steps.

I. INTRODUCTION

Complementary Metal-Oxide-Semiconductor (CMOS) power management integrated circuits are indispensable in modern electronic systems. For example, 5 V MOS-Field Effect Transistors (MOSFET) are typically based on 0.18 μm technology.^{1,2} For power electronics, it is important to increase carrier mobility to reduce on-state resistance (R_{ON}) while maintaining a good safe-operating-area (SOA). It should be noted that a power transistor is in linear regime (low drain-source voltage, V_{DS}) when it acts as a power switch. Therefore, R_{ON} depends on the inversion carrier low-field mobilities. It is well-known that the inversion carrier mobility, μ , in Silicon MOSFETs follows the universal curve^{3,4} when plotted against effective vertical electric field, $E_{\perp}$, regardless of substrate doping concentration³ or gate oxide thickness.⁴ The inversion layer mobility, μ , is a result of three scattering mechanisms, Coulomb scattering by ionized impurities, μ_C , phonon scattering, μ_{ph} , and surface roughness scattering, μ_{sr} , related by Matthiessen's rule,³

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}}. \quad (1)$$

The dominant scattering mechanism changes from Coulomb scattering at low vertical fields to temperature dependent phonon scattering at moderate vertical electric fields, due to the screening effect induced by inversion charges. The dominant mechanism at high vertical fields is non-temperature-dependent surface roughness scattering due to the confinement of inversion carriers close to the Si/SiO₂ interface by the triangular potential.

The oxygen-insertion (OI) Si channel MOSFET has been shown to improve R_{ON} among other critical figures of merit in MOSFETs. OI Si channel MOSFETs are so-called be-

cause they include the insertion of partial monolayers of oxygen atoms during the epitaxial growth of the uppermost region of the silicon substrate, near the gate dielectric (Fig. 1). The gate oxide quality of an OI-MOSFET is found to be better than that of a standard MOSFET. For example, it has a lower direct tunneling gate leakage,⁵⁻⁷ less negative bias temperature instability (NBTI),⁸ and higher time-dependent dielectric breakdown (TDDB).⁷ Particularly, we have shown that an OI-nMOSFET has a higher inversion electron mobility than a standard nMOSFET because its electron μ_{sr} is 53% higher than the universal curve.⁹ Improvement in μ_{sr} , which dominates at high gate overdrive, is essential to the reduction of R_{ON} because power switches are usually biased with high gate overdrive at on-state.

The improvement of OI-MOSFET gate dielectric (including both poly-Si/SiON₃ and high- κ -metal-gate stacks^{6,8}) is believed to be due, at least in part, to an exchange of oxygen atoms between the OI layer and the gate oxide during annealing. The exchange of oxygen between the OI layer and the gate oxide is evident from an isotope labeling experiment.¹⁰ Hence, the electron mobility improvement is likely due to a change in Si/SiO₂ interface roughness.

To further study the origin of electron μ_{sr} improvement in OI-MOSFET, in this paper, transmission electron microscopy (TEM) pictures of the transistors are taken to study the Si/SiO₂ interface roughness and SiO₂ oxide thickness variations in OI-MOSFETs compared to standard MOSFETs. Then, OI-pMOSFETs and standard pMOSFETs are fabricated, and the hole inversion layer mobilities are extracted and deconvolved using cryogenic measurement as in Refs. 9 and 11. It is found that hole inversion mobility is similar in OI-MOSFET and standard MOSFET. To explain the difference in electron and hole mobility improvements, the power spectral density (PSD) of Si/SiO₂ interface roughness is extracted,

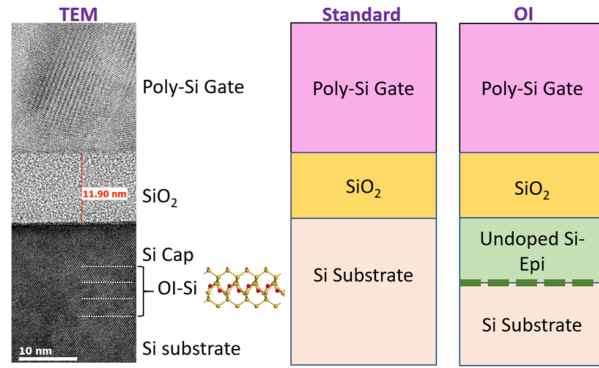


FIG. 1. Left: TEM picture of the gate stack being studied. The gate oxide thickness is about 11.9 nm. The TEM picture of this resolution cannot distinguish OI-MOSFET (MST) from standard MOSFET (STD) devices. Oxygen Inserted Si layers are located under 5nm away from the gate oxide interface. Middle and right: Illustrations of the gate/channel stack of the baseline standard MOSFET (STD) device (middle) and the OI-MOSFET (MST) device (right). The OI layers are represented as a dashed line.⁹

and μ_{sr} is calculated numerically.

II. DEVICE FABRICATION AND EXPERIMENTAL SETUP

The fabrication of the OI- and standard pMOSFETs is similar to that of the corresponding nMOSFETs detailed in Ref. 9. It has a p^+ poly-Si/SiO₂ gate stack and is fabricated in the same commercial 5 V 0.18 μ m technology as the nMOSFETs with an OI option. The OI-Si channel was formed during selective Si epitaxy on active-patterned 200 mm wafers by intermittently exposing the Si surface to a dilute oxygen source. Note that besides being a standard in 5 V power technology, the p^+ poly-Si/SiO₂ gate stack also simplifies the study over the high- κ gate stack, which will introduce additional scattering mechanisms and complicate the analysis. Two wafers were fabricated for comparison, a standard wafer dubbed as "pSTD" and an OI wafer called "pMST". Figure 1 shows the general gate stack structure employed for the fabrication. The standard wafer, "pSTD", contains the standard pMOSFETs and was fabricated using the baseline process, which consisted of a chain Arsenic and Phosphorus implantations (multi-energy, multi-dose sequence) followed by a well RTA (1050°C, 5 s) targeting a threshold voltage of $V_{th} = -0.7$ V. The non-standard wafer containing the OI-pMOSFETs, "pMST6", was fabricated using the same process as used in "pSTD" except that an epitaxial layer containing four oxygen partial monolayers followed by a 13 nm undoped Si epitaxial capping layer, which allowed for 7 nm Si consumption during pre-gate clean and gate oxidation to obtain a 6 nm final Si cap, was selectively grown after high temperature. The well implant dose and annealing in the "pMST" wafer were also adjusted to have a similar maximum depletion width, and thus similar minimum depletion capacitance as the "pSTD" wafer (Fig. 2). The gate oxide thickness is

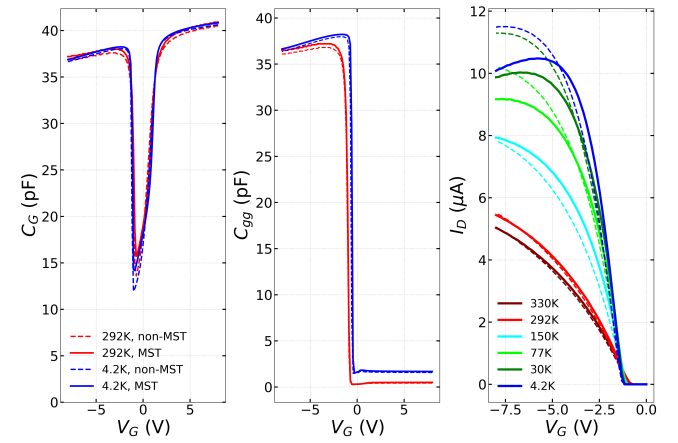


FIG. 2. The full-CV (left), split-CV (middle), and I_D - V_G (right) curves measured at various temperatures. Dashed lines are standard p-type MOSFET (non-MST) - "pSTD" wafer and solid lines are p-type OI MOSFET (MST) - "pMST" wafer. For clarity, only 292 K and 4.2 K are shown in the CV curves. $V_D = -50$ mV in the I_D - V_G measurement.

about 12 nm.

III. PMOSFET MEASUREMENT RESULTS AND MOBILITY EXTRACTION

Large area transistors ($W = 120$ μ m and $L = 120$ μ m) were used for accurate capacitance-voltage (CV) and gate voltage-drain current (I_D - V_G) measurements. They were measured from 300 K to 4.2 K using a Lakeshore TTPX probe station system with four arms. Liquid Helium was used to cool down the sample, with the temperature controlled by a Lakeshore Model 336 temperature controller. The temperatures were monitored by three sensors at the sample, probe arm, and radiation shield, respectively. The temperature reported below refers to the reading at the sample.

For the I_D - V_G measurement, the drain voltage, V_D , was set to -50 mV, and the gate voltage, V_G , was swept from 0 V to -8 V using Keysight E5262A IV Analyzer. For the CV measurement, both full-CV and split-CV were measured using Keysight E4980A LCR meter at 100 kHz with 25 mV small signal amplitude and long integration. V_G was swept from -8 V to 8 V. In the full-CV measurement, the drain, source, and body were grounded, and it was performed for a sanity check to ensure the measurement was normal at various temperatures and for the verification of the maximum depletion width. For the split-CV measurement, it was the same as the full-CV measurement except that the body was allowed to float to enable an accurate extraction of the inversion charge for mobility calculation. It should be noted that for the low inversion regime, a measurement frequency lower than 100 kHz might be desirable to reduce the influence of the channel resistance on the accuracy^{12,13} However, 100 kHz is used because the high inversion regime is of higher interest and 100 kHz is less affected by the noise associated with slow traps in CV measurements.

Figure 2 shows the CV characteristics of the standard pMOSFET and OI-pMOSFET at 292 K and 4 K. No significant difference between the two samples is observed for all the temperatures. Figure 2 also shows the $I_D - V_G$ curves at $V_D = -50$ mV. It shows that they have similar currents from 4.2 K to 77 K. However, at lower temperatures, the $I_D - V_G$ curves of OI-pMOSFET exhibit negative differential resistance (NDR) at high V_G . This is due to the increase in surface roughness scattering as phonon scattering is negligible at low temperatures as discussed in Ref 9. This indicates that OI-pMOSFET hole μ_{sr} is similar to that of the standard pMOSFET at the normal operating voltage, but is lower at very high operating voltage. This is different from n-type MOSFETs in Ref. 9.

Following the approach in Refs. 3 and 9, the hole inversion mobility is deconvolved into Coulomb, phonon, and surface roughness scattering components according to Matthiessen's rule given in Eq. (1). The empirical expressions for each scattering mechanism are

$$\mu_{sr,pSTD} = 140E_{\perp}^{-1.3}, \quad (2)$$

$$\mu_{sr,pMST} = 120E_{\perp}^{-1.55}, \quad (3)$$

$$\mu_{ph} = 3.3 \times 10^5 T^{-1.4} E_{\perp}^{-0.2}, \quad (4)$$

$$\mu_C = A_C Q_I^2. \quad (5)$$

where $\mu_{sr,pSTD}$ and $\mu_{sr,pMST}$ are the μ_{sr} of the standard pMOSFET (pSTD) and OI-pMOSFET (pMST), respectively. Equation (5) is an empirical model for Coulomb scattering, which captures the screening effect by the inversion electrons. Here, A_C is a temperature-dependent but field-independent prefactor, and Q_I is the inversion charge density. For consistency, all mobilities in Eqs. (2)-(5) are reported in cm^2/Vs , with $E_{\perp}$ expressed in MV/cm and Q_I in cm^{-2} . The effective vertical electric field ($E_{\perp}$) is calculated using $E_{\perp} = (|V_G| + 1.5|V_{th}|)/(7.5t_{ox})$, where V_G is the applied gate voltage, V_{th} is the threshold voltage, and t_{ox} is the gate oxide thickness.⁴

The extracted total mobility is well described by Matthiessen's rule using these scattering terms. As shown in Fig. 3, there is a good agreement between the empirical model and experimental data, thereby validating the deconvolution approach. Strain effects can be excluded as the origin of the mobility improvement in the OI-Si channel. Strain is known to modify phonon scattering through changes in the sub-band structure; however, the temperature-dependent mobility component is modeled using the same formulation for both the OI-Si channel and the standard Si channel control, indicating no observable strain-induced modification of phonon scattering. Furthermore, the in-plane strain in the OI-Si channel extracted from UV-Raman peak shifts was as small as $-0.034\% \pm 0.038\%$ biaxial tensile strain (equivalent to -116 ± 30 MPa biaxial tensile stress), while the strain along the depth direction obtained from angle-dip High-Resolution Rutherford backscattering spectrometry (HR-RBS) measurements remained within the measurement error ($< 0.18\%$).¹⁴ These results indicate that strain effects are negligible and therefore do not account for the observed mobility enhancement. It is found that, compared to standard pMOSFETs, OI-pMOSFETs exhibit higher μ_{sr} when $E_{\perp} < 0.6$ MV/cm

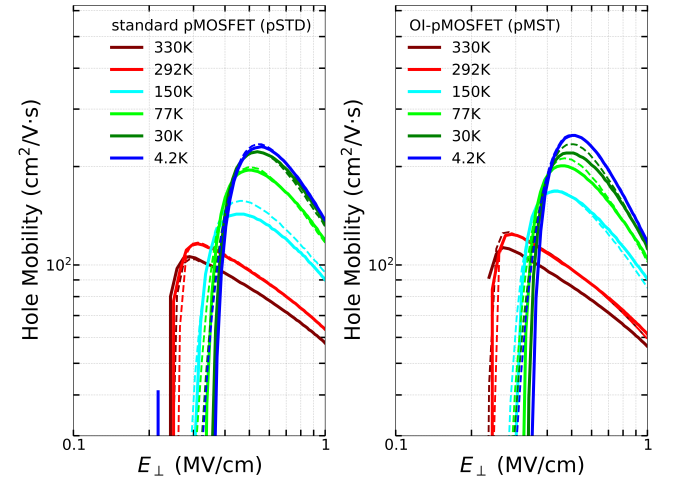


FIG. 3. Hole mobility as a function of temperature and $E_{\perp}$ for the standard pMOSFET "pSTD" (left) and OI-pMOSFET "pMST" (right) devices. Solid lines are the mobilities extracted using the $I_D - V_G$ and split-CV curves. Dashed lines are fitting curves using Eqs. (1)-(5).

($V_G \approx 4$ V) but smaller μ_{sr} at higher $E_{\perp}$. This agrees with the observation in Fig. 2.

IV. INTERFACE ROUGHNESS ANALYSIS

The difference in nMOSFETs and pMOSFETs μ_{sr} trends cannot be explained by purely arguing that the OI-MOSFETs have a smoother Si/SiO₂ interface. Based on the study in Ref. 15, one might need to understand the relationship between the Si/SiO₂ interface roughness PSDs and the Fermi level of the inversion carriers to explain the inconsistency. More specifically, if the PSDs of the OI-MOSFETs and the standard MOSFETs have a crossover and if the electron (hole) Fermi level is at the region where the OI-MOSFET PSD is smaller (larger) than the standard MOSFET PSD, then it can explain the observation.

Therefore, TEM pictures at the gate oxide region were taken for both OI-MOSFET and standard MOSFET for Si/SiO₂ interface roughness PSD calculations. Seven TEM pictures were taken at the same device, and each covers a domain of about 51 nm. The gate/oxide (top) and oxide/substrate (bottom) interfaces were identified and digitized using two different weighted intensity thresholds. One has 50% at the other regions and 50% at the oxide (dubbed "50-50"). The other has 75% at the other regions and 25% at the oxide (dubbed "75-25"). The SiO₂ oxide thickness is calculated from the distance between the top and the bottom interfaces, while the Si/SiO₂ interface roughness is extracted by digitalizing the bottom (oxide/substrate) interface. The sampling of the digitalized interface was performed at uniform intervals of 0.055 nm, corresponding to a spatial sampling frequency of 18.18 nm^{-1} . Figure 4 shows one of the TEM images with the interfaces identified using the two schemes. Figure 5 shows the calculated oxide thickness and extracted Si/SiO₂ interface

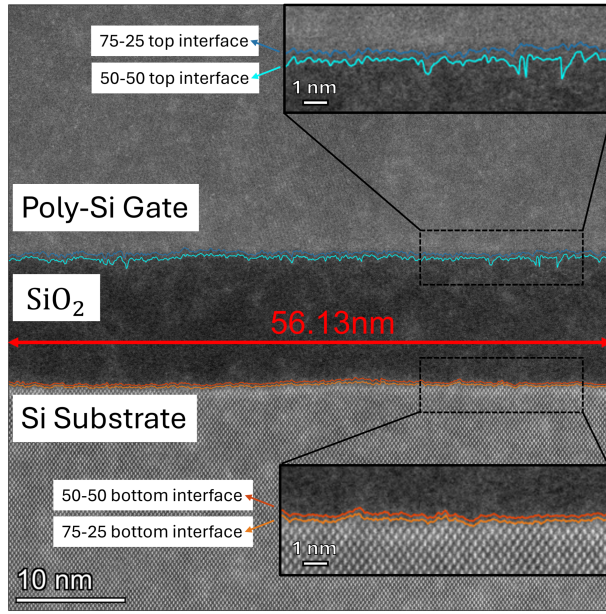


FIG. 4. TEM image of a standard pMOSFET device showing the interface boundaries extracted using the "75-25" and "50-50" intensity thresholds. These boundaries are used as the reference for oxide thickness and interface roughness calculations in Fig. 5.

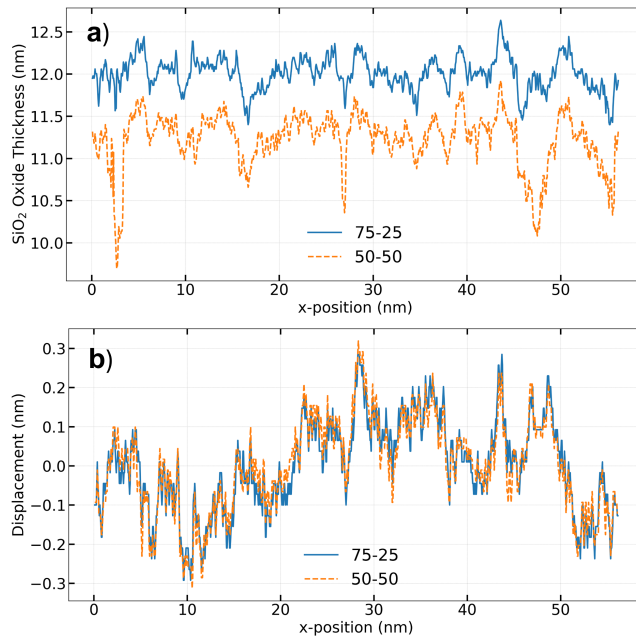


FIG. 5. (a) Oxide thickness and (b) Si/SiO₂ interface roughness extracted from TEM sample using two different boundary conditions: the "75-25" intensity threshold and the "50-50" threshold. The Si/SiO₂ interface roughness is calculated at the bottom Si/SiO₂ interface by finding the displacement from the average interface location as shown in Fig. 4.

roughness for the different boundary conditions. The "75-25" boundary scheme produced oxide thickness in line with the expected 12 nm value, and was therefore adopted for Si/SiO₂ interface roughness extraction and subsequent PSD analysis.

PSD, $S(q)$ where q is a reciprocal vector, is defined as the Fourier transformation of the autocorrelation function of the root-mean-square (rms), $\Delta(r)$ where r is the distance vector, of the interface roughness.^{15,16} The $S(q)$ is usually assumed to be a function like Gaussian¹⁷ or exponential and fitted using correlation length against an AR-based PSD.¹⁸ The assumed forms, like Gaussian and exponential, of the autocorrelation function are fitted by including roughness parameters, roughness rms value (Δ), and correlation length (Λ). Depending on the form assumed for the $S(q)$, the value of the roughness parameters can change, making it hard to choose what form to assume for the $S(q)$.¹⁹ Another method proposed is to directly compute $S(q)$ using FFT-based PSD or fit the $S(q)$ using an AR-based PSD.¹⁵ However, FFT-based PSD exhibits fluctuations and is not smooth compared to AR-based PSD.^{15,18}

An autoregressive (AR) PSD approach has been previously used to characterize interface roughness and extract surface roughness scattering-limited mobility in unstrained and strained Si MOSFETs.¹⁵ A similar approach is used in this paper by finding the corresponding one-dimensional power spectral density of the Si/SiO₂ interface roughness from the TEM line scans using a sixth-order Yule-Walker autoregressive model.^{18,20}

In the autoregressive (AR) modeling approach, the Si/SiO₂ interface profile is represented as a linear combination of its previous M samples,

$$\alpha(n) = h(n) + \gamma_1 h(n-1) + \gamma_2 h(n-2) \cdots + \gamma_M h(n-M) \quad (6)$$

where $\alpha(n)$ denotes the prediction error, while $h(n)$ is the actual measured variable at the same position. The coefficients $\gamma_1, \gamma_2, \dots, \gamma_M$ are the AR prediction error filter coefficients.

The AR-based PSD is calculated using the AR-based power spectrum formula^{18,20}

$$S(q)^{\text{AR}} = \frac{\sigma_a^2}{|1 + \sum_{n=1}^M \gamma_n e^{-iqn\delta_x}|^2} \quad (7)$$

where σ_a^2 is the prediction error variance of the AR process, δ_x is the scan resolution, and $M = 6$ is the model order used for this paper. As shown in Fig. 6, a 6-th order AR-based PSD of the Si/SiO₂ interface roughness is much smoother than a FFT-based one.

The PSDs of the seven Si/SiO₂ interface roughness of each device are averaged and shown in Fig. 7. Both interface extraction schemes were used. There are two observations. Firstly, "75-25" and "50-50" have similar shapes, and their OI- and standard-MOSFET $S(q)$ have a similar relationship. Secondly, for both schemes, OI-MOSFET has a smaller PSD at low spatial frequency regimes and a higher PSD at some high spatial frequency regimes. This can likely explain the different behavior in nMOSFET and pMOSFET μ_{sr} . In the following analysis of μ_{sr} , the PSDs extracted for OI- and standard devices are applied to both nMOSFET and pMOSFET of the corresponding type. This assumes that PSD is defined

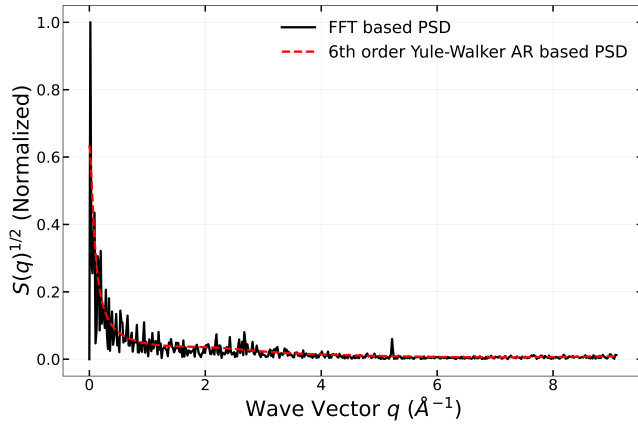


FIG. 6. Comparison of FFT-based PSD and sixth-order Yule-Walker AR-based PSD of the Si/SiO₂ interface roughness of one of the TEM line scan of a standard MOSFET device.

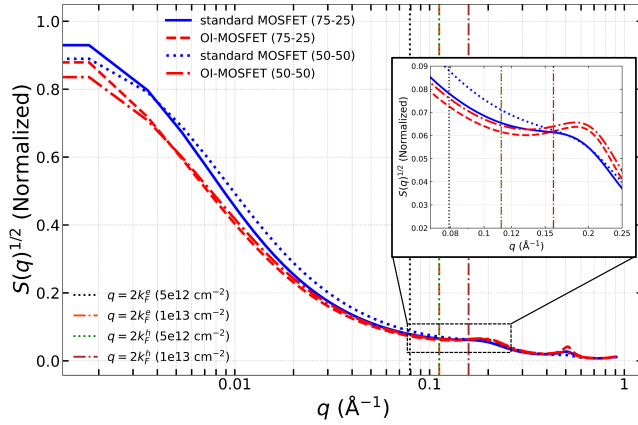


FIG. 7. Averaged Si/SiO₂ interface roughness AR-based PSDs for OI and standard MOSFET devices, extracted using the “75–25” and “50–50” boundary conditions. The normalized square-root PSD, $S(q)^{1/2}$, is plotted for comparison between OI-MOSFETs (MST) and standard MOSFETs (Non-MST). Vertical lines indicate $q = 2k_F$, calculated at inversion charge densities of $N_{inv} = 5 \times 10^{12} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$. These are denoted as k_F^e and k_F^h for electrons and holes, respectively. Distinct line styles — black dotted and orange dash-dot for $q = 2k_F^e$, and green dotted and maroon dash-dot for $q = 2k_F^h$ — differentiate between carrier types, and the N_{inv} values are given in parentheses.

by the process (OI- vs. standard process). Given that “75–25” extracted the oxide thickness closer to the expected value, it will be used in the following analysis.

To gain physical insight into how interface roughness influences μ_{sr} for electrons and holes in both OI- and standard devices, the power spectral density (PSD) (Fig. 7) is examined within a physically relevant inversion charge density range of $N_{inv} = 5 \times 10^{12} \text{ cm}^{-2}$ to $1 \times 10^{13} \text{ cm}^{-2}$, where surface roughness scattering is known to be a dominant mobility-limiting mechanism in MOSFETs.²¹ Since carriers near the Fermi level dominate roughness-limited scattering, the corresponding spatial frequency $q = 2k_F$ becomes the most rel-

evant in the $S(q)$.^{15,21} Here, k_F is the Fermi wave vector, which is directly related to the inversion charge density N_{inv} by $k_F = \sqrt{2\pi N_{inv}/g_0}$, where g_0 is the subband degeneracy factor—equal to 2 for electrons and 1 for holes. The difference in g_0 gives rise to different $q = 2k_F$ values for electrons and holes for the same N_{inv} . Accordingly, PSD values at $q = 2k_F$ serve as a meaningful basis for interpreting differences in μ_{sr} between electrons and holes in both OI- and standard nMOSFET and pMOSFET.

Figure 7 presents the PSD spectra for OI- and standard devices, computed using the “75–25” Si/SiO₂ interface roughness extraction scheme. Vertical lines indicate the spatial frequencies $q = 2k_F$ corresponding to inversion charge densities (N_{inv}) of $5 \times 10^{12} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$, calculated using $k_F = \sqrt{2\pi N_{inv}/g_0}$, where $g_0 = 2$ for electrons and $g_0 = 1$ for holes. In Fig. 7, these are denoted as k_F^e and k_F^h for electrons and holes, respectively, with distinct line styles. These q values reflect the dominant wavevectors involved in roughness-limited scattering.^{15,21} Across this range, the MST nMOSFET shows lower PSD than the non-MST counterpart, implying reduced roughness scattering and a higher μ_{sr} . In contrast, PSDs for OI- and standard pMOSFETs remain nearly identical for the range of values, indicating similar μ_{sr} . More importantly, it should be noted that the OI-pMOSFET PSD becomes faintly larger at a higher N_{inv} . This explains the larger reduction in OI-pMOSFET μ_{sr} than the standard pMOSFET in Fig. 3 and Eq. 3 at high $E_{\perp}$. This range-based comparison highlights the role of Si/SiO₂ interface roughness PSD ($S(q)$) in determining μ_{sr} differences between OI-MOSFET (MST) and standard MOSFET (non-MST) devices across nMOSFET and pMOSFET. To further understand the relationship between the PSDs and μ_{sr} , numerical calculations are required to link the measured PSD to carrier mobility. Previous studies have shown that top-interface roughness can complicate the potential fluctuations associated with roughness scattering in thin gate dielectrics when the top and bottom interfaces are not correlated, since oxide-thickness fluctuations introduce additional scattering components.^{22,23} This effect is particularly significant when the SiO₂ thickness is much smaller than 100 Å. The normalized cross-correlation between the top and bottom interfaces was evaluated as

$$R_{tb}(\tau) = \frac{\langle \delta z_t(x) \delta z_b(x + \tau) \rangle}{\sigma_t \sigma_b}, \quad (8)$$

where $\delta z_t(x)$ and $\delta z_b(x)$ denote the roughness fluctuations of the top and bottom interfaces, respectively, σ_t and σ_b are their root-mean-square roughness values, and τ represents the lateral shift. In the present study, the extracted peak correlation value of 0.8725 at $\tau = 0 \text{ nm}$ indicates that the interfaces are well correlated and that the top interface fluctuations have a minimal impact on the mobility analysis.

V. NUMERICAL CALCULATION OF SURFACE ROUGHNESS SCATTERING MOBILITY

To evaluate the impact of Si/SiO₂ interface roughness on carrier transport, a basic understanding of carrier mobility is

required. The general surface roughness scattering limited mobility is given by $\mu_{sr} = e\langle\tau_m\rangle/m^*$, where m^* is the conductivity effective mass and τ_m is the momentum relaxation time. The average of the momentum relation time over all occupied states, $\langle\tau_m\rangle$, can be found using

$$\langle\tau_m\rangle = \frac{\int_{E_0}^{\infty} \tau_M(E) \frac{\partial f_0}{\partial E} (E - E_0) dE}{\int_{E_0}^{\infty} f_0 dE} . \quad (9)$$

where f_0 is the Fermi distribution function, and E_0 is the lowest subband energy. Carriers close to the Fermi level are the ones that contribute heavily to the surface roughness scattering. The surface roughness-limited mobility μ_{sr} is then found out to be:^{3,15,21}

$$\frac{1}{\mu_{sr}} = \frac{e m_d m_c E_{\perp}^2}{\pi \hbar^3} \int_0^{2\pi} (1 - \cos \theta) S(q) d\theta . \quad (10)$$

where e is the elementary charge, $\hbar$ is the reduced Planck constant, and m_d and m_c are the density-of-states and conductivity effective masses, respectively. The wave vector q is defined as $q = 2k_F \sin(\theta/2)$, with $k_F = \sqrt{2\pi N_{inv}/g_0}$ being the Fermi wave vector and θ being the scattering angle. Here, N_{inv} is the inversion charge density extracted from split-CV measurements, and g_0 is the subband degeneracy (2 for electrons, 1 for holes).

The integral in (10) relates μ_{sr} directly to the power spectral density $S(q)$ of the interface, which contains the information of the spatial frequency content of Si/SiO₂ interface roughness.

From the experiment, the $E_{\perp}$ -dependent μ_{sr} for OI- and standard MOSFETs have been extracted as in Eqs. (2) and (3) for pMOSFETs in this paper and Eqs. (12) and (13) for nMOSFETs in Ref. 9. They are all in the following form,

$$\mu_{sr} = K E_{\perp}^{-n} . \quad (11)$$

with where K and n are fitting parameters extracted from device characterization measurements. The best-fit equations for the SR mobility are repeated below:

$$\mu_{sr, nSTD} = 850 E_{\perp}^{-2} , \quad (12)$$

$$\mu_{sr, nMST} = 1300 E_{\perp}^{-2} , \quad (13)$$

$$\mu_{sr, pSTD} = 120 E_{\perp}^{-1.3} , \quad (14)$$

$$\mu_{sr, pMST} = 140 E_{\perp}^{-1.55} . \quad (15)$$

Figure 8 presents the experimentally extracted surface roughness mobility (μ_{sr}) versus the effective vertical field ($E_{\perp}$) for OI- and standard devices, based on the fitted expressions in Eqs. (12)–(15).⁹ The OI-nMOSFET shows a clear enhancement in μ_{sr} compared to the standard nMOSFET, indicating reduced surface roughness scattering. In contrast, the pMOSFETs show minimal difference between OI- and standard device types, suggesting no notable change in hole

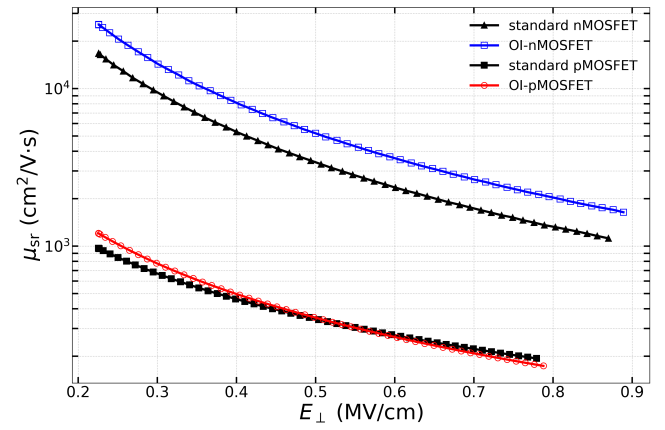


FIG. 8. Experimental SR mobility from Eqs. (12) to (15) vs $E_{\perp}$ for OI- and standard nMOSFETs and pMOSFETs.

μ_{sr} . These experimental observations provide the need for the study on μ_{sr} based on the power spectral density ($S(q)$) of the Si/SiO₂ interface roughness using Eq. (10).

To simplify the calculation of μ_{sr} and ease of comparing μ_{sr} between OI- and standard devices, it is assumed that the OI- process does not affect the density-of-states effective mass (m_d) or the conductivity effective mass (m_c), which are taken to be the same for OI and standard devices for each type of carrier (electron and hole).

To calculate surface roughness scattering-limited mobility, Eq. (10) is numerically computed using the calculated $S(q)$ spectra. The integration is carried out over the scattering angle θ , with the wavevector (q) related to θ as $q = 2k_F \sin(\theta/2)$, where $k_F = \sqrt{2\pi N_{inv}/g_0}$. For each inversion charge density N_{inv} , the corresponding effective vertical field $E_{\perp}$ is obtained from split-CV measurements, thereby establishing a mapping between $S(q)$ and $E_{\perp}$ via N_{inv} . The resulting μ_{sr} is then calculated using a modified form of Eq. (10):

$$\frac{1}{\mu_{sr}} = C \cdot E_{\perp}^2 \int_0^{2\pi} (1 - \cos \theta) A \cdot S(q) d\theta . \quad (16)$$

where $C = (e m_d m_c)/(\pi \hbar^3)$ is a prefactor containing physical constants and effective mass parameters: e is the elementary charge, $\hbar$ is the reduced Planck constant, and m_d , m_c are the density-of-states and conductivity effective masses of carriers, respectively.

In Eq. (16), the measured PSD $S(q)$ is not directly substituted into the integral. Instead, it is scaled by a scaling factor 'A' to correct for the dimensional mismatch between the 1D PSD obtained from TEM line scans (units: nm³) and the 2D PSD required in Eq. (10) (units: nm⁴). Dimensional analysis of Eq. (10) shows that $S(q)$ carries units of nm⁴, characteristic of a 2D PSD as the surface is two-dimensional. Although mathematical techniques exist to convert 1D PSDs into 2D representations, these rely on assumptions about the surface profile, such as isotropy, or involve complex transformations.²⁴ Here, a simple scaling factor A is introduced to scale the magnitude of $S(q)$. Moreover, as mentioned in Ref. 15, a correction factor should be applied as the

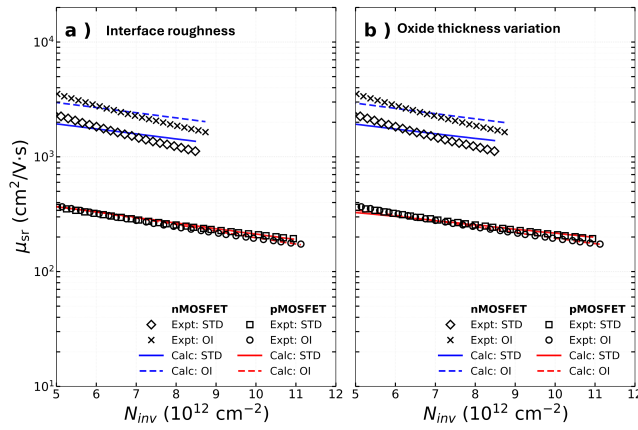


FIG. 9. Surface roughness mobility (μ_{sr}) as a function of inversion carrier density (N_{inv}) for standard (STD) and oxygen-inserted (OI) MOSFETs. Experimental (Expt.) data are shown as black markers ($\diamond$, $\times$ for nMOSFETs; $\square$, $\circ$ for pMOSFETs), while calculated (Calc.) values are represented by colored lines (blue = electrons, red = holes; solid = STD, dashed = OI). (a) μ_{sr} calculated using the Si/SiO₂ interface roughness power spectral density (PSD). (b) μ_{sr} calculated using the SiO₂ oxide thickness variation PSD. All calculations employ the 75–25 boundary scheme.

extracted interface roughness is affected by the TEM sample thickness (projecting effect). This factor is also absorbed in A in this study.

The best-fit values of A were found by matching the calculated μ_{sr} from Eq (16) to the experimental curves shown in Fig. 8 (but converted the x-axis to N_{inv} in the range of interest mentioned earlier). This fitting yields $A = 6.5$ for OI-nMOSFET, $A = 92$ for OI-pMOSFET, $A = 8.5$ for the standard nMOSFETs, and $A = 80$ for the standard pMOSFETs. These parameters are obtained from the fitting procedure described above and are applied in the numerical calculations to reproduce the experimental μ_{sr} trends for both interface roughness and oxide thickness variation analyses. The comparison between calculated and experimental μ_{sr} for OI- and standard devices is shown in Fig. 9. The numerical calculation matches the experimental trends well. Firstly, the mobility difference between OI-nMOSFET and standard-nMOSFET is larger than that of pMOSFET. Moreover, at high N_{inv} , the difference between OI-pMOSFET and standard-pMOSFET is much smaller, which agrees with the experimental trend.

To provide a more quantitative comparison of the mobility enhancement, Fig. 10 shows the mobility enhancement factor, defined as $\mu_{sr}^{OI}/\mu_{sr}^{STD}$, as a function of inversion carrier density (N_{inv}) for both nMOSFETs and pMOSFETs. Experimental results and numerical calculations are plotted together to directly compare the enhancement trends. The experimental data show a significantly larger mobility enhancement for nMOSFETs than for pMOSFETs, while the calculations reproduce the overall trend and capture the relative difference between carrier types. In particular, the enhancement factor for pMOSFETs approaches unity at higher N_{inv} .

Although the PSD of Si/SiO₂ interface roughness is used in the calculations of μ_{sr} as given in Eq. 16, a similar explanation

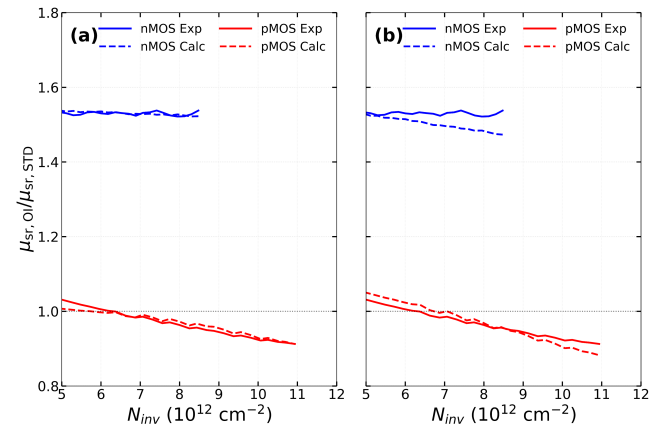


FIG. 10. Mobility enhancement factor ($\mu_{sr}^{OI}/\mu_{sr}^{STD}$) as a function of inversion carrier density (N_{inv}) for nMOSFETs and pMOSFETs. Solid lines represent experimental data, while dashed lines show calculated results. (a) Enhancement factor derived from calculations based on Si/SiO₂ interface roughness PSD. (b) Enhancement factor derived from calculations based on oxide thickness variation PSD.

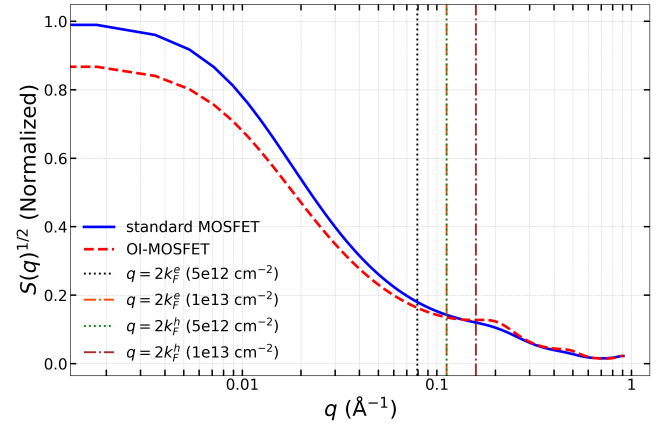


FIG. 11. Averaged SiO₂ oxide thickness variation AR-based PSDs for OI and standard devices, with vertical lines indicating ($q = 2k_F$) calculations at inversion charge densities of $N_{inv} = 5 \times 10^{12} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$. These are denoted as k_F^e and k_F^h for electrons and holes, respectively. Distinct line styles—black dotted and orange dash-dot for $q = 2k_F^e$, and green dotted and maroon dash-dot for $q = 2k_F^h$ —help differentiate between carrier types, and N_{inv} levels values are in the parentheses.

can be obtained by considering oxide thickness variations. After obtaining the oxide thickness profile from TEM line scans, the average thickness of the profile is subtracted to get oxide thickness variation data.²⁵ The PSD of oxide thickness variations can be extracted by using the same methods applied to the Si/SiO₂ interface roughness. Such oxide thickness variations can change the mobility of the carrier because this results in vertical electric field variations and, thus, confinement triangular well variations. Figure 11 presents the PSD for oxide thickness variations for OI- and standard MOSFET devices, computed using the "75-25" boundary scheme. Vertical lines mark the spatial frequencies $q = 2k_F$, corresponding to an N_{inv}

of $5 \times 10^{12} \text{ cm}^{-2}$ and $1 \times 10^{13} \text{ cm}^{-2}$, with $k_F = \sqrt{2\pi N_{inv}/g_0}$, where $g_0 = 2$ for electrons and $g_0 = 1$ for holes. These values, denoted k_F^e and k_F^h , show the dominant wavevectors influencing surface roughness scattering and, hence, μ_{sr} . Across this range, the OI-nMOSFET exhibits a lower oxide thickness variation PSD compared to the standard MOSFET, indicating a higher μ_{sr} . By contrast, the OI- and standard pMOSFETs exhibit nearly identical oxide thickness variation PSDs, with the OI-pMOSFET PSD becoming slightly larger at higher spatial frequencies. This explains the behavior of why OI-pMOSFET shows no improvement in μ_{sr} and even a lower μ_{sr} at higher $E_{\perp}$. The scaling factor A for oxide thickness variation PSDs for OI-MOSFET was found to be $A = 1.4$ for n-type and $A = 21$ for p-type, for the standard MOSFETs $A = 1.7$ and $A = 18.5$ for n and p type, respectively. The final calculated μ_{sr} using oxide thickness variation and experimental μ_{sr} for standard and OI-MOSFET devices is shown in Fig. 9.

VI. OXYGEN TRACER EXPERIMENTS

To investigate the physical mechanism for the surface roughness reduction of the OI-Si channel, oxygen transport during thermal processing was traced by growing the OI-Si film using an ^{18}O isotope precursor. Figures 12 (a), (b), and (c) show ^{18}O and ^{16}O Secondary ion-mass spectrometry (SIMS) profiles after epitaxial OI-Si film growth, after 800°C wet oxidation process, and after post-oxidation anneal in N_2 ambient at 800°C for 20 minutes, respectively. After the oxidation process, a small hump of ^{18}O can be seen at the oxide/silicon interface. The dose of this peak matches well with the change in ^{18}O dose of the as-grown OI-Si film. After the post-oxidation anneal, dose of the ^{18}O peak is increased by a factor of 5. In return, ^{16}O dose in the OI Si film is increased by 50% after the oxidation process, and by 150% after the post-oxidation anneal, respectively. These changes clearly show the presence of dynamic oxygen exchange process between the gate dielectric and the OI-Si film during thermal processing. Since the oxygen exchange is a kinetic process, it suggests a possibility of improving hole mobility by further tuning thermal process conditions.

VII. CONCLUSION

Oxygen-insertion (OI) silicon technology has shown enhanced surface-roughness-limited mobility in bulk nMOSFETs compared with conventional silicon channels. However, this improvement is not observed in pMOSFETs. Power spectral density (PSD) analysis—based on TEM imaging and numerical simulations—reveals that the Fermi wave vectors of electrons and holes occupy different regions of the PSD spectrum. The electron Fermi wave vector lies in a low-frequency range where the OI-PSD is lower than that of the standard device, leading to improved mobility. In contrast, the hole Fermi wave vector falls within a high-frequency range where the OI and standard PSDs are similar, resulting in negligible mobility gains. An oxygen tracer experiment identified a dynamic

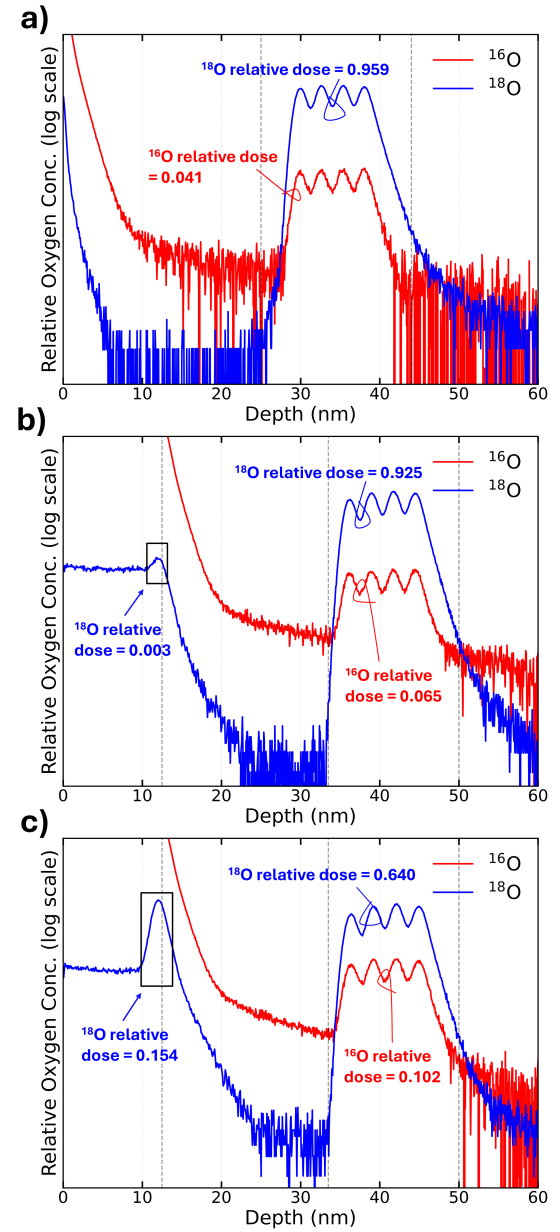


FIG. 12. ^{18}O and ^{16}O SIMS profiles (a) OI-Si epitaxial growth; (b) after 800°C wet oxidation; (c) after post-oxidation anneal at 900°C for 20 minutes.

exchange process between the Si/ SiO_2 interface and the OI-Si layer. These findings suggest that SRS-limited hole mobility in OI-Si pMOSFETs could be improved via engineering of post-oxidation processing steps. The improved surface roughness scattering on the OI-Si channel demonstrated in this study also opens up an opportunity for improving the performance of high-k/metal-gate (HKMG) stack for bulk and fully depleted silicon-on-insulator (FDSOI) planar CMOS technology nodes that uses thermally grown SiO_2 as an interfacial layer (IL). Since the improvement of surface roughness scattering in the OI-Si channel is attributed to dynamic exchange

of oxygen atoms between OI-Si and SiO₂, fine tuning of thermal processing of post-oxidation step is expected to improve surface roughness for HKMG stack using thermal interfacial layer.

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DATA AVAILABILITY STATEMENT

Non-confidential data is available upon reasonable request.

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